
MARCH 1978
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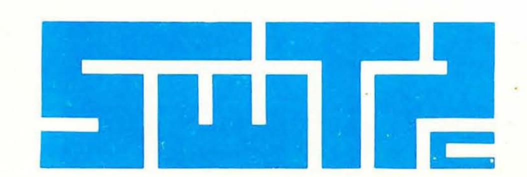
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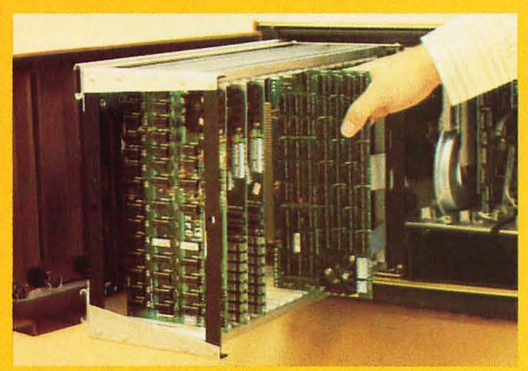


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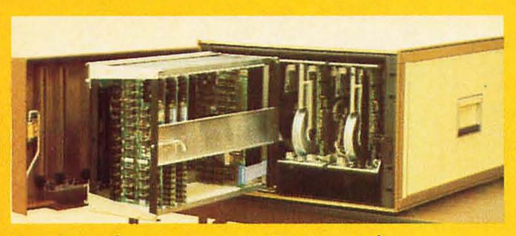
MORE ABOUT THE SYSTEM THREE . . .



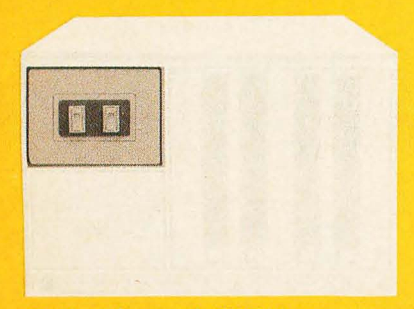
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BYTE March 1978
Volume 3 Number 3

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Nucleus

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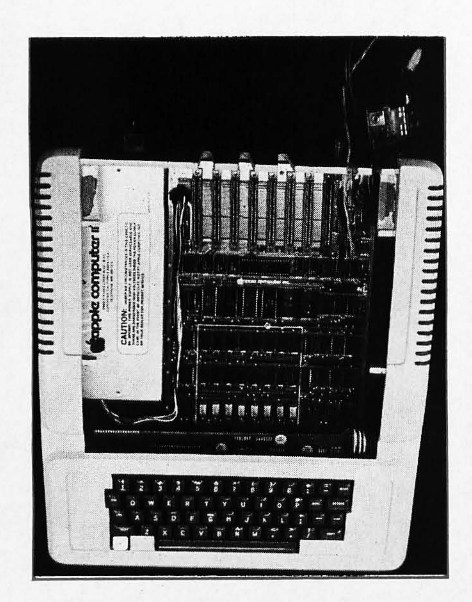
In This BYTE

About the Cover. . .

This month, Robert Tinney has created an oil painting on the theme of "Organs of Computers." Two articles in this issue concern the prospect of using a personal computer system for the editing and playing of music using pipe organs under electronic control, a prospect which is emphasized by the typical small system in place of the organist. A grand pipe organ facade and red carpet emphasize the regal nature of this king of instruments — with its new servant the small computer.

The Soloworks lab at the University of Pittsburgh has been conducting experiments with computers for some time. One of their areas of interest is computer music. Jeffrey Lederer, Tom Dwyer and Margot Critchfield of that organization describe their experiments with pipe organs and a new high level music language called MUSIC in **A Two Computer Music System.** *Page 8*

The Apple II is one of several examples of fully assembled "appliance" computers available coast to coast off the shelf in computer stores. Read **An Apple to Byte** for a user's reations to this product, and an example of a simple "color sketchpad" application implemented on the Apple II. *Page 18*



If you don't know your Rauschepfeife from your Holtzregal, perhaps **The Microcomputer and the Pipe Organ** by Jef Raskin can help. The article introduces readers to pipe organ technology and gives valuable advice to the enterprising experimenter who wants to experiment with programmed passacaglias on a Grossemischung. *Page 56*

The study of biological neural computers is an important input to thought and design of robotic systems. This issue contains Ernest W Kent's third article in a series on **The Brains of Men and Machines.** This installment, **How the Brain Analyzes Input,** gives essential background information on the organization and operation of sensory processing in the nervous systems of mammals such as man. *Page 74*

Would you like to do your own EROM programming, but don't know how to begin? Read Steve Ciarcia's **Program Your Next EROM in BASIC.** You'll find an inexpensive circuit for programming and erasing these useful devices. *Page 84*

We have seen advance publicity and claims about the PET 2001 by Commodore for some time now. In this issue, Dan Fylstra reports on the realities of **The PET 2001** which arrived at his door October 11 1977. *Page 114*



In part 2 of his 3 part series on **CIE Net: A Design for a Network of Community Information Exchanges,** Mike Wilber presents the detailed protocols designed for various types of messages between users and between intelligent nodes of the network itself. *Page 152*

Readers of the January 1978 BYTE may recall Dark Horse, one of the computer program contenders for the World Computer Chess Championship. This month, Peter Jennings' Microchess program makes a valiant effort to beat the favorite in **Microchess 1.5 versus Dark Horse.** *Page 166*

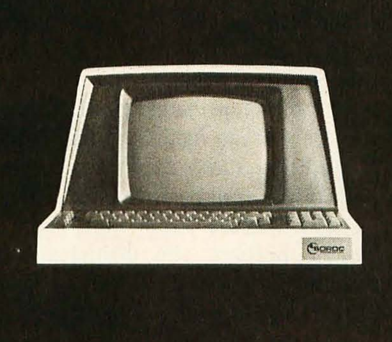
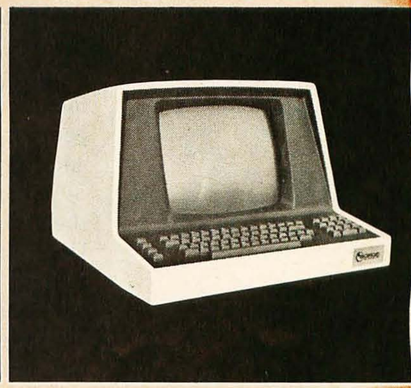
Have you ever thought you might like to **Take a Course in Microprogramming?** Richard Mac Millan gives his reactions upon taking such a course from the Wintek Corporation. His information may help you decide if the course you think you might like to take is just what you had in mind. *Page 168*

A really useful microcomputer should be able to control the environment around it. To do this it must be capable of controlling electronic devices which are not TTL compatible. Hank Olson describes several ways of doing this in **Controlling the Real World.** *Page 174*

A mass storage system is essential to the truly usable personal computer. One option for obtaining mass storage is presented in this issue by Phil Hughes' article **Interfacing the Sykes OEM Floppy Disk Kit to a Personal Computer.** *Page 178*

With the cost of microprocessors so low, the barriers to a multiprocessor capability go down. Rather than adding a memory region to your system, why not consider the concept of adding a combined memory and microprocessor subsystem. With an appropriate multiport memory region and control logic, Ken R Castleman's **The Intelligent Memory Block** is a very real possibility for the homebrewer with higher thruput as a goal. *Page 186*

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Don't Ignore the High End

. . .or My Search for Manuscript Editing Paradise

by Carl Helmers

In this issue, we have included the first two of four users' reviews of fully assembled and tested self-contained computers. The selection criterion is that the "typical user" (in two cases Dan Fylstra, one case Dennis Barbour, and one case myself) was able to purchase an off-the-shelf computer of the low end "appliance" variety. These machines represent a significant technological achievement in the form of a fairly inexpensive computer with a high level language (BASIC) and limited mass storage facility in the form of audio or modified audio cassette tape. In their class of price and performance circa December 1 1977, these "appliance" computers represent perhaps the ultimate we have seen to date.

As time goes on, I'll update the ultimate, but that is not my purpose in this essay. There is a utilitarian class of personal computer products which I have used most in my homebrew system. I refer of course to the high end of performance in small computer systems, the system with perhaps 16 K to 32 K memory, single or dual full size floppy disks, terminal device, and all the accoutrements of what we used to know as "minicomputers" but now within the price range of the family that can afford an $8000 car. My attention was turned to this class of machine recently when I began shopping around for some equipment and software to automate several aspects of the manuscript preparation process which I and my associates in the editorial department perform daily at BYTE.

Continued on page 136

Some Enticing Advance Words

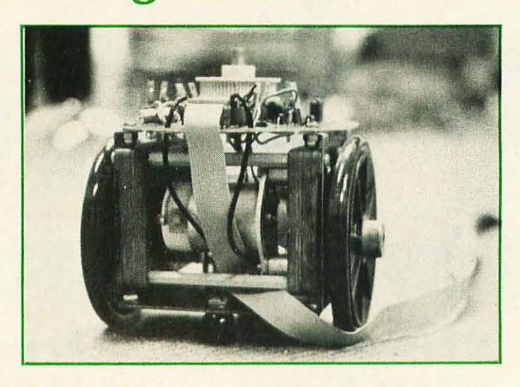


Photo 1.

Turtles are coming. In mid November 1977, Dan Hillis of the LOGO project at Massachusetts Institute of Technology called BYTE and posed one of those questions which have only one answer. "Would readers of BYTE magazine be interested in an inexpensive kit version of the famous LOGO project turtle robots?" Dan outlined on the phone the idea of a kit with a target price of $250, and suggested that I take a trip to the MIT AI (artificial intelligence) Laboratory to take a look at his prototypes. I was delighted to accept the invitation, which included a heady tour of some of the projects at the AI laboratory and the Architecture Machine project's advanced color video display technology.

The turtle is not yet ready for market, but it is getting close, as can be seen by photo 1 which I took while lying prone on the floor of the laboratory as Dan put the prototype through its paces. The idea is to produce a rugged and childproof motion output device with tail drag plotting capabilities provided by a ball point pen controlled by solenoid. In the past turtle robots have proved to be excellent devices for teaching children programming concepts, both in simulations on screens, and as mechanically mobile output peripherals. The intent is to make the new turtle product virtually indestructible with Lexan plastic housing and wheels, and rugged mechanical and electronic innards. Dan demonstrated some of this indestructibility with a prototype sans housing by dropping it from a height of about two meters onto the carpeted floor of the laboratory.

Of course a turtle is not all hardware, so versions of the LOGO language adapted to personal computer architectures will be required. Dan and his associates (all quite young) at MIT have formed a company which intends to introduce turtles much more formally sometime in early 1978. We'll expect to keep readers informed of this exciting prospect as it develops and gets closer to production.■



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A Two Computer Music System

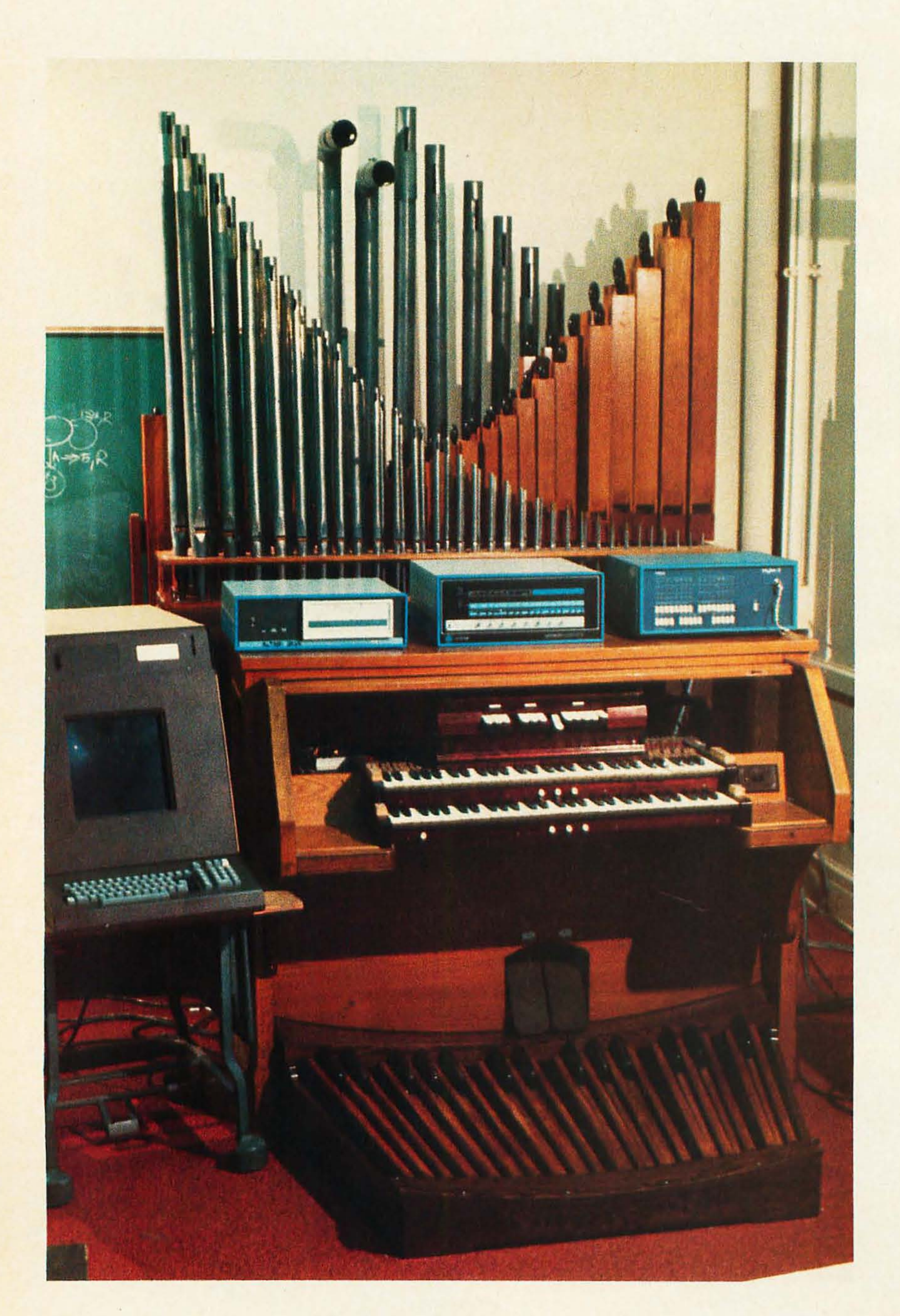


Photo 1: The authors' overall system with graphics terminal on the left and the disk drive and two computers on top of the organ console. The wooden pipes at top right are the flute rank; the metal pipes are a viola rank. The stop tablets for selecting ranks and harmonics can be seen just above the top keyboard.

The music system described here started out a few years ago as a project in the Soloworks Lab. The idea was to put together a "manipulable" system that allowed students to work with the powerful mathematical idea of *synthesis*. We felt that mathematics and science students should be able to experience firsthand what could be done by superimposing components that worked together to synthesize some bigger concept.

Real, full-blown professional music seemed like an ideal metaphor for working with this "superimposition" principle. It's easy for a student to see that a musical performance is really a multitude of small, discrete events working in perfect synchronism. But it's even easier to sense that the resultant whole is greater than the sum of its parts. In fact, the "whole" can be a human experience of quite thrilling proportions.

The system that evolved has met this goal very well. Students of varied backgrounds are able (and motivated) to work patiently with complex scores, making the final performance a proof of the power of the principle of superimposition.

But a funny thing happened on the way to this goal. The total system began to look more and more like a "micro" computer science curriculum. The documentation that evolved began to contain much of the jargon that permeates computing, but this seemed to be easier to take when interpreted in terms of the friendlier worlds of music and art.

In writing this condensed description of the system, we therefore decided to leave the jargon in. Our purpose is to not only describe the music system but to suggest that interesting new approaches to teaching computer science might be developed along similar lines. There is equally good promise for teaching computer science subject matter in terms of visual art. Abstract games are another fruitful area. It's probably no coincidence that all these examples illustrate the kind of computing most people would call "fun." There's undoubtedly a deep educational lesson lurking here, but that's another subject.

Jeffrey H Lederer
Tom Dwyer
Margot Critchfield
Project Solo
University of Pittsburgh
Pittsburgh PA 15260

Why a Pipe Organ?

The system described here is general enough to apply to a variety of musical instruments. It was implemented with a small pipe organ because this illustrates the general kind of performance ensemble used by composers who write orchestral works. A pipe organ has several sets of pipes called *ranks*, each set having a distinctive tonal characteristic called timbre. The ranks are selected by pressing switches called *stop tablets*, so that an organist is able to control an entire "orchestra" of sounds by using different stop settings. Further, since most pipe organs have several keyboards (often including one for the feet), the ranks can be played independently. Thus both chorded (several notes played simultaneously) and contrapuntal (independent melody lines played simultaneously) music can be played on one or more keyboards.

The organ is also the original "synthetic music" instrument. This is because a performer can add harmonics to fundamental tones by pressing suitable stop tablets. When the stop tablet marked "8 foot flute" is pressed, one gets flutelike sounds, in the normal register (where A=440 Hz). (The phrase "8 foot" comes from the fact that the largest pipe in the rank is eight feet high.) But when the stop marked "4 foot flute" is pressed, everything sounds an octave higher. If *both* stops are activated, we then have a sound rich in second harmonics. Traditional organs have stops labeled "8 foot," "4 foot," "2 2/3 foot," "2 foot," etc. However, the stop settings in the computer system described here are software generated, so any harmonic can be specified (of course there are only a finite number of pipes available for playing these harmonics).

Overview of the System

The Music System uses two microcomputers (an Altair 8800b system and an Intellec 8/MOD 80), a small pipe organ, and a Magnavox plasma display graphics terminal. Figure 1 shows how these components are interconnected.

In addition to the hardware, there are three software packages. The first is a graphics music editor that allows a composer to "draw" his score on a graphics display terminal. The editor converts the graphic representation of the score into a MUSIC language program. The program may also be created and edited using a standard text editor, in which case an alphanumeric terminal can be used. Either type of editor is run on the master system. The MUSIC language programs can be saved on a diskette as files.

Before a MUSIC language program can be played, it must be "compiled." Our compiler is a program that accepts MUSIC language programs as input, and outputs an annotated listing of the MUSIC language program along with error messages and an "object" program. The object program consists of instruc-

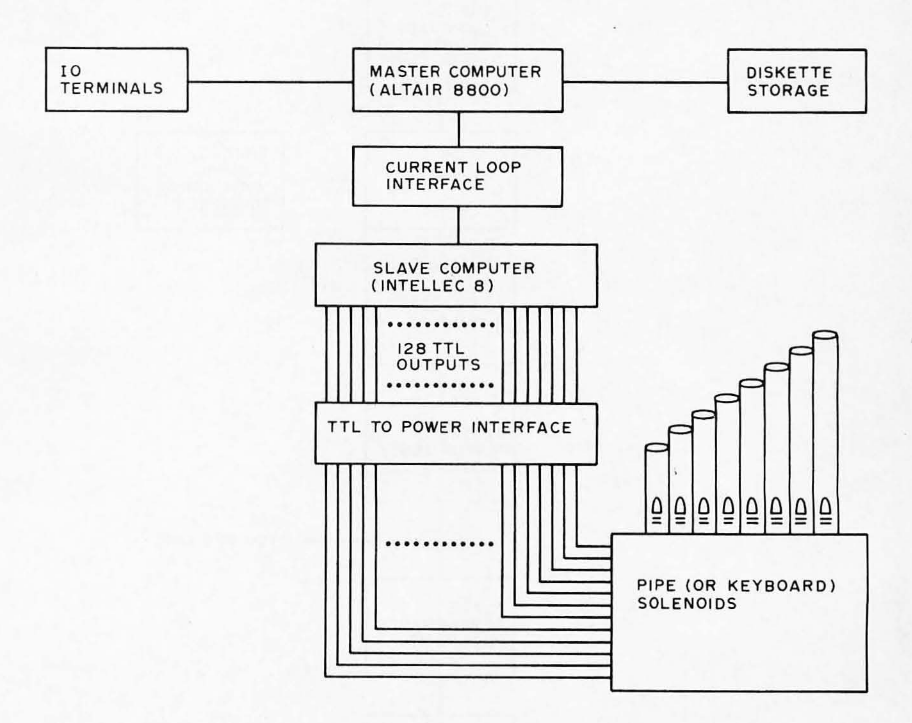


Figure 1: Hardware components of the authors' computerized organ music system. This design requires one TTL output line for each pipe to be controlled.

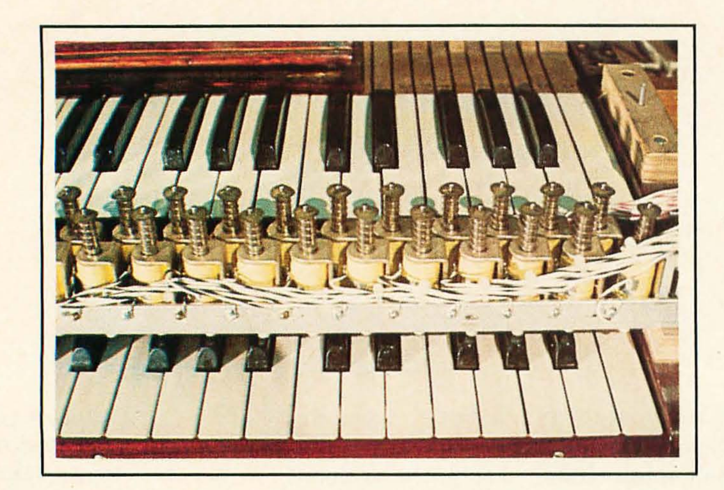


Photo 2: A set of solenoids used to automatically play the keys. Since this setup plays the keys directly, it could be easily adapted to any standard keyboard instrument including harpsichord and piano.

COMPOSER

GRAPHICS TERMINAL

ALPHANUMERIC TERMINAL

EDITOR

MUSIC LANGUAGE SOURCE FILE

COMPILER

SOURCE LISTING WITH ERROR MESSAGES

OBJECT FILE

MASTER PERFORMANCE PROGRAM

2400 BPS LINE

SLAVE PERFORMANCE PROGRAM

PIPE ORGAN

Figure 2: Software block diagram of the computer organ music system.

tions which are easily interpreted by the slave computer. The compiler runs on the master computer.

The object program is "played" using both computers. First, the object program is transferred from the master to the slave computer. The slave computer executes the object program in order to drive the pipe organ. A pair of programs (one on each computer) controls the transfer of the object program and its execution. Figure 2 shows the relationship between software components.

System Hardware

The slave microcomputer is an Intellec 8/MOD 80 with 8 K bytes of programmable memory, 2 K bytes of read only memory containing a system monitor program, 256 bytes of programmable read only memory that contains the second performance program, 16 latching output ports, and a serial bidirectional IO port. Each latching port is eight bits wide, with each bit dedicated to controlling a pipe valve of the organ. Thus, $16 \times 8 = 128$ pipes can be controlled. The interface between each pipe and its controlling port is a Darlington switching transistor connected as shown in figure 3.

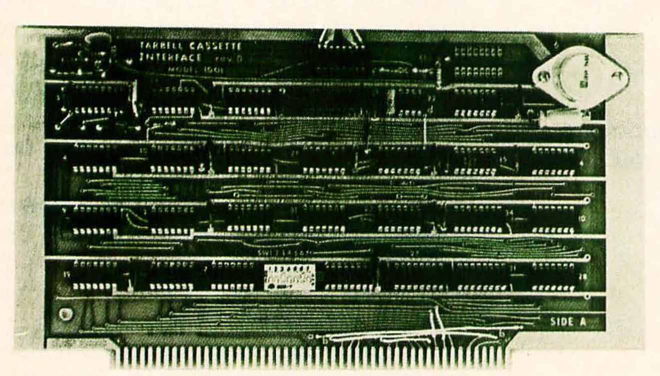
The master computer is an Altair 8800b with 60 K bytes of memory, two diskette drives and two serial ports. One serial port is used as the console line and is connected to a Magnavox plasma graphics terminal. This terminal has a plasma display with 512 by 512 dots. A character generator is used to display 32 lines of 64 characters; the characters can be either a set of standard ASCII characters or a user loaded set (musical symbols in our case). The terminal has a vector generator and dot addressability. Sections of the screen can be selectively erased and written. The graphics terminal is optional, and there is no reason why other lower cost graphics displays couldn't be used if appropriate changes in software were made. The Intecolor 8001 might be particularly appropriate since different colors could be used to distinguish voices in polyphonic music.

The second serial line connects the Altair to the Intellec over a 2400 bps current loop. A special interface had to be built to isolate the two active current loops. The schematic is shown in figure 4.

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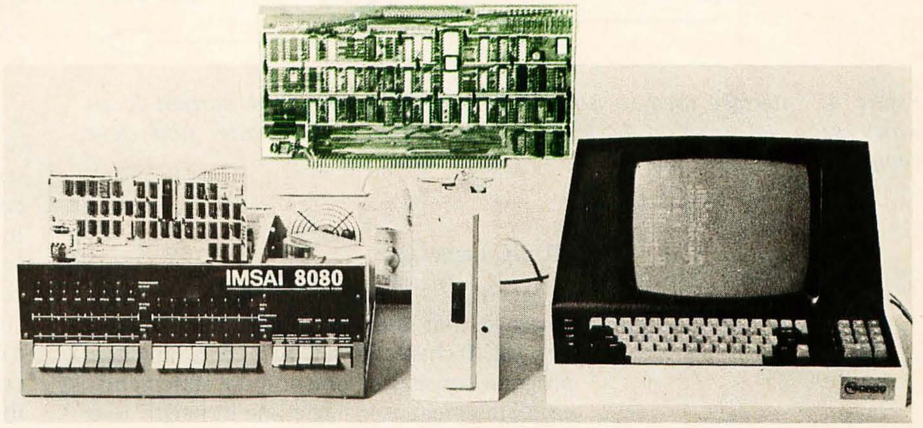


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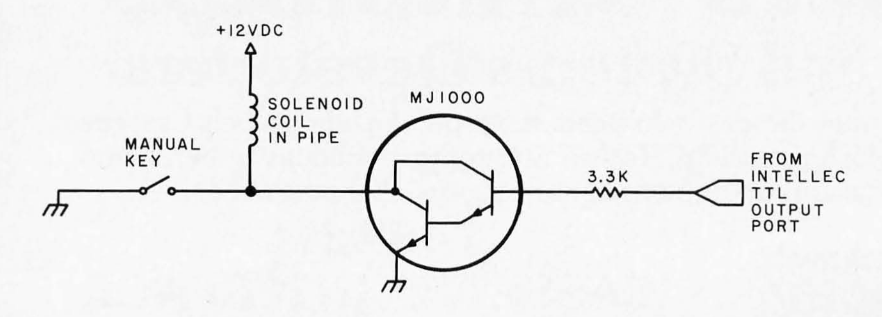


Figure 3: Interface between an organ pipe solenoid and a computer output bit. One such circuit is needed for each pipe to be controlled in this design. The solenoid in each pipe opens a valve that admits air to the pipe.

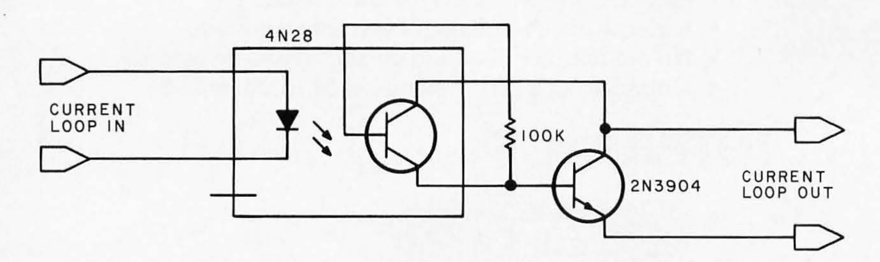


Figure 4: Interface used to isolate the two 2400 bps active current loops which send information back and forth between the master and slave computers.

MUSIC Language

MUSIC is a high level music notation language that uses the standard 64 character ASCII character set. A MUSIC language program consists of one or more statements; each statement is a single line in length (see figure 5 and listing 1).

There are three types of statements in this language: command, data, and comment statements. Comment statements, which begin with two asterisks, may be placed anywhere in the program; they are ignored by the compiler.

The command statements consist of a single asterisk followed by the command mnemonic and the command's parameters. The commands in this language are divided into three categories: delimiter commands, repeat commands, and context commands.

The delimiter commands separate measures (BAR), parts of measures (CHANGE), and mark the end of the last measure of the program (END). The parameters of the first two commands, when used, set a temporary time signature for a measure.

The repeat commands control the repetition of sections of the score. The limits of a repeated section are bracketed by HEAD and TAIL commands. When necessary, each separate ending of a repeated section starts with an ENDING command, and sections of a score between SIGN commands can be skipped the second time through a repeated section. Repeated sections can be nested within each other.

The context commands are used to change the condition under which the notes of the program are compiled. These commands set the key signature (KEY), time signature (TIME) and metronome setting with or without accelerandos and ritards (TEMPO). A special context command (STOPS) controls the number of voices allowed in each measure and the stop (timbre) settings for each voice.

The notes for a MUSIC language program are placed in the data statements. Each data statement consists of one or more events; each event is separated from the previous event by a semicolon. An event is a note, chord, glissando, tremolo or rest. The notes can be played with different articulations (staccato, legato, or normal). *[See the glossary at the end of this article.]* Each data statement contains the events to be performed by one voice during a single measure or fraction of a measure.

A normal measure of music consists of a starting BAR command followed by zero or more context commands and one data statement for each active voice. When a context change occurs inside a measure, the form of that measure is slightly different. In this case the measure starts with a BAR command, zero or more context commands and one data statement for each voice. These data statements contain those events that occur before the context change. Following the data statements is a CHANGE command, one or more context commands and one data statement for each voice. These latter data statements contain the events that occur after the context change. Repeat commands may be intermixed with the context commands of a measure.

The voices in each measure are performed concurrently. Each voice is assigned a group of stop settings. Each stop setting takes a note, displaces it a set amount of tones, and assigns that new pitch to a given rank of pipes. Multiple stop settings for a voice will generate multiple pitches for each note in an event. These pitches are played simultaneously. The number of voices and their stop settings are controlled by the STOPS command.

This all sounds pretty complicated, but new users quickly get proficient with the language. Having all the features of musical notation available has proven to be well worth the extra complexity.

Continued on page 48

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TI is into personal computers in a big way, and that means a ground floor opportunity is going to be open for you, the personal computing innovator. You'll be joining the undisputed world leader in creating new products and markets for consumer electronics with the company that invented the calculator on a chip. And it's all going to happen in TI's new Management and Technology Center for Consumer Products in Lubbock, Texas. Located in the high, dry, and cool plains of West Texas, Lubbock is about halfway between Dallas and Albuquerque. It is the home of Texas Tech University. You are just a few hours' drive from skiing in Taos, or touring and shopping in Juarez, Mexico.

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Opportunity to design and develop digital subsystems for major new products. Projects will require design-to-cost discipline with internal and external component vendors, vendors of peripheral devices and making trade-offs of hardware and software. Requires BSEE with 2 years' experience. Prefer experience in design of bubble and/or flexible disk computer memory subsystems.

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Letters

NETWORKING WITH TELEPHONES?

Dave Caulkins' Personal Computer Network (PCNET), in September 1977 BYTE, sounds like a great idea, for those who live in the Palo Alto CA area; but until PCNET goes national or semi-national there is a method available (on a smaller scale) to computer users right now: Northwestern Bell's Direct Dial Conferencing. Using DDC, up to six computers can exchange data using standard Touch-Tone telephones and modems. For complete instructions and to see if DDC is available in your area contact your local Northwestern Bell business office. There is only one problem with using DDC, it costs $.50 per minute. That can add up to quite a lot in a short amount of time, if you're not careful!

Another way to do the same thing at a fraction of the cost is by using another gadget that Ma Bell provides, Three Way Calling. You can get Three Way Calling (if it's available in your area) simply by asking for it and paying about $2.50 per month additional on your phone bill. With Three Way Calling you and two friends can exchange data without a costly per minute charge. The number of computers you can interface together might be increased by the use of Three Way Calling by more than one of the persons involved. I have not had the opportunity to try this, so I can't guarantee anything. Perhaps there is no limit to how far you can go.

Steve Hughes
4410 Douglas Av S
Golden Valley MN 55416

BACKLIGHTING VIA PHOTOCOPY

With all of the comments that I have seen about the advantages of using backlighting for reading PAPERBYTES, it is rather suprising that I have not seen the following suggestion for accomplishing it without wasting magazine space: let those readers who wish to use the backlighting method photocopy the appropriate pages. The photocopies could then be read by backlighting as they would only be printed on one side. Obviously, though, the photocopies would have to be of the highest quality. From what I have seen of the coin operated machines and home type machines, they would not be of sufficient quality, but that obtained at copying centers probably would be.

I will admit that I have not tried this idea, primarily because my system is not yet operational. However, I think it is an idea well worth trying.

Clark Jones
225 Pennsylvania NE Apt H
Albuquerque NM 87108

Fred Merkowitz of Micro-Scan Associates, Natick MA, reports that his front side scanner works just fine with photocopies of bar codes, sometimes tried through several generations of recopying just to see what would happen. Backlighting is just not needed with an appropriate scanner.

COMMENTS ON PROGRAMMING AND DESIGN STYLE

I would like to thank David A Higgins for his article "Structured Program Design" (October 1977 BYTE, page 146); however, I found that his presentation lacked clarity. There are a large number of reasons why "top-down" structured programming became popular. I feel that Mr Higgins has misapplied his design technique, in the same way he feels top-down programming was misapplied to design.

The Warnier-Orr diagrams approach to design should, I feel, be followed (and augmented) by the top-down approach to programming. What happens when a design technique is applied directly to coding is shown clearly by Mr Higgins' own programming example! He claims that the resultant code is easy to read and understand. I stipulate that this is only true if the programmer working on it has the original Warnier-Orr diagram it was coded from. This same argument applies to his next two points as well. A program is easy to change and maintain only if the program logic flow is immediately evident. If we were to draw lines between all of Mr Higgins' GOSUBs and their destinations, we would end up with another bowl of cold spaghetti! Again, the documentation he has consists mainly of a title remark at the head of each subroutine, which serves only to relate each subroutine to a bracket in the Warnier-Orr diagram.

Continued on page 128

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AZ: Tempe: Byte Shop, 813 N. Scottsdale, (602)894-1129; Phoenix: Byte Shop, 12654 N. 28th, (602)942-7300; Tucson: Byte Shop, 2612 E. Broadway, (602)327-4579. **CA:** Berkeley: Byte Shop, 1514 University, (415)845-6366; Citrus Heights: Byte Shop, 6041 Greenback, (916) 961-2983; Costa Mesa: Computer Center, 1913 Harbor, (714)646-0221; Hayward: Byte Shop, 1122 "B" St., (415)537-2983; Lawndale: Byte Shop, 16508 Hawthorne, (213)371-2421; Orange: Computer Mart, 633-B W. Katella, (714) 633-1222; Pasadena: Byte Shop, 496 S. Lake, (213)684-3311; Sacramento: Micro-Computer Application Systems, 2322 Capitol, (916) 443-4944; San Francisco: Byte Shop, 321 Pacific, (415)421-8686; San Jose: Byte Shop, 2626 Union, (408)377-4685; San Rafael: Byte Shop, 509 Francisco, (415)457-9311; Tarzana: Byte Shop, 18423 Ventura, (213)343-3919; Walnut Creek: Byte Shop, 2989 N. Main, (415)933-6252. **CO:** Boulder: Byte Shop, 3101 Walnut, (303) 449-6233. **FL:** Ft. Lauderdale: Byte Shop, 1044 E. Oakland Pk., (305)561-2983; Miami: Byte Shop, 7825 Bird, (305)264-2983; Tampa: Microcomputer Systems, 144 So. Dale Mabry, (813)879-4301. **GA:** Atlanta: Computer Mart, 5091-B Buford, (404)455-0647. **IL:** Champaign: Computer Co., 318 N. Neil, (217)359-5883; Numbers Racket, 623½ S. Wright, (217)352-5435; Evanston: itty bitty machine co, 1322 Chicago, (312)328-6800; Lombard: itty bitty machine co, 42 W. Roosevelt, (312)620-5808. **IN:** Bloomington: Data Domain, 406 S. College, (812) 334-3607; Indianapolis: Data Domain, 7027 N. Michigan, (317)251-3139. **IA:** Davenport: Computer Store, 4128 Brady, (319)386-3330. **KY:** Louisville: Data Domain, 3028 Hunsinger, (502)456-5242. **MI:** Ann Arbor: Computer Store, 310 E. Washington, (313)995-7616; Troy: General Computer Store, 2011 Livernois, (313) 362-0022. **MN:** Minneapolis: Computer Depot, 3515 W. 70th, (612)927-5601. **NJ:** Hoboken: Computer Works, 20 Hudson Pl., (201)420-1644; Iselin: Computer Mart, 501 Rt. 27, (201)283-0600. **NY:** New York: Computer Mart, 118 Madison, (212)686-7923; White Plains: Computer Corner, 200 Hamilton, (914)949-3282. **NC:** Raleigh: ROMs 'N' RAMs, Crabtree Valley Mall, (919) 781-0003. **OH:** Columbus: Byte Shop, 2432 Chester, (614)486-7761; Dayton: Computer Mart, 2665 S. Dixie, (513)296-1248. **OR:** Beaverton: Byte Shop, 3482 SW Cedar Hills, (503)644-2686; Eugene: Real Oregon Computer Co., 205 W. 10th, (503)484-1040; Portland: Byte Shop, 2033 SW 4th Ave., (503)223-3496. **RI:** Warwick: Computer Power, M24 Airport Mall, 1800 Post Rd., (401)738-4477. **SC:** Columbia: Byte Shop, 2018 Green, (803)771-7824. **TN:** Kingsport: Microproducts & Systems, 2307 E. Center, (615)245-8081. **TX:** Arlington: Computer Port, 926 N. Collins, (817)469-1502; Houston: Computertex, 2300 Richmond, (713)526-3456; Interactive Computers, 7646½ Dashwood, (713)772-5257; Lubbock: Neighborhood Computer Store, 4902-34th St., (806)797-1468; Richardson: Micro Store, 634 So. Central Expwy., (214)231-1096. **VA:** McLean: Computer Systems Store, 1984 Chain Bridge, (703)821-8333; Virginia Beach: Home Computer Center, 2927 Va. Beach Blvd., (804)340-1977. **WA:** Bellevue: Byte Shop, 14701 NE 20th, (206)746-0651; Seattle: Retail Computer Store, 410 NE 72nd, (206)524-4101. **WI:** Madison: Computer Store, 1863 Monroe, (608)255-5552; Milwaukee: Computer Store, 6916 W. North, (414)259-9140. **D.C.:** Georgetown Computer Store, 3286 M St. NW, (203)362-2127. **CANADA:** Ottawa, Ont: Trintronics, 160 Elgin, (613)236-7767; Toronto, Ont: Computer Mart, 1543 Bayview, (416) 484-9708; First Canadian Computer Store, 44 Eglinton Ave. W., (416)482-8080; Computer Place, 186 Queen St. W., (416)598-0262; Vancouver, B.C.: Basic Computer Group, 1438 E. 8th, (604)736-7474; Pacific Computer Store, 4509 Rupert, (604)438-3282.

Processor Technology

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Seven points to consider before you buy your small computer.

In this magazine, alone, there are probably a dozen ads for small computers. New companies are breaking ground like spring flowers.

How, then, do you determine which computer offers the features you need most... at the price you can afford?

We'd like to propose seven basic questions to help you make an intelligent decision.

1. How complete is the computer system?

Many buyers of small computers are in for a rude awakening when they have to spend additional money for interfaces.

The Sol-20 Terminal Computer was the first *complete* small computer system. Everything you need to make it work is included in the basic package.

2. Is powerful system software available?

It won't do if your system is "tongue-tied."

Processor Technology Corporation has devoted more effort to the development of software than any other small computer maker. Our latest offering is the first fully implemented disk operating system for a small computer: PTDOS. It contains over 40 major commands, several languages and numerous utilities. Our high level languages include Extended BASIC, Assembler, FORTRAN,* FOCAL and PILOT.*

3. Is the system easy to expand?

More and more computer owners are expanding their small computers to handle business and other specialized requirements.

The largest Sol system can handle 64K bytes of RAM memory and operate with a three megabyte on-line disk memory. Sol systems use the S-100 Bus. So you can use a wide variety of hardware.

*Available soon.

4. Is the computer well-engineered?

Our Sol systems are the most conservatively rated and ruggedly built in the industry, period. In addition we designed them with you, the user, in mind; Sols are easy to build and a joy to operate.

5. Does it have proven reliability?

What is the track record? There are over 5,000 Sol systems in the field. Our track record for reliable performance is unparalleled in the small computer field.

6. Does it have good factory support?

A computer is a complex piece of hardware. So you want to be sure it is backed up with complete manuals, drawings and a factory support team that cares.

Processor Technology offers the most extensive documentation of any small computer manufacturer. And we maintain a patient, competent telephone staff to answer your questions.

7. Are maintenance and service people accessible?

Where are they located?

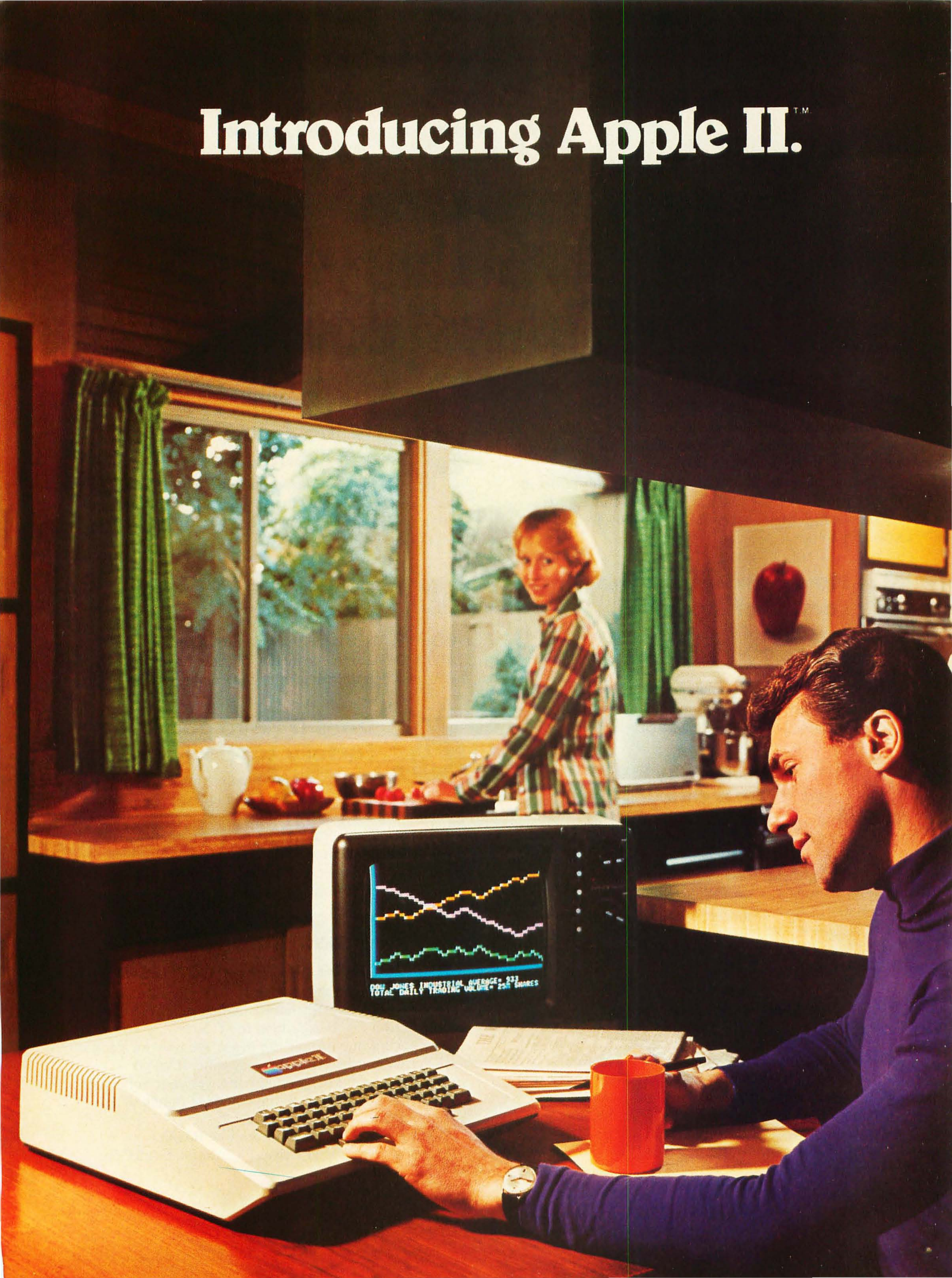
Processor Technology has maintenance and service people in over 50 cities around the U.S.

As you continue turning the pages, see how we stack up to the other computers in this magazine. If we've succeeded in whetting your appetite, see your Sol dealer or write for information on the complete family of Sol computers.

Processor Technology Corporation, Box B,
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Processor Technology

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Introducing Apple II.™

The home computer that's ready to work, play and grow with you.

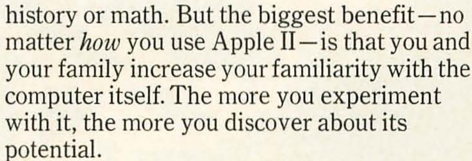
Clear the kitchen table. Bring in the color T.V. Plug in your new Apple II,* and connect any standard cassette recorder/player. Now you're ready for an evening of discovery in the new world of personal computers.

Only Apple II makes it that easy. It's a complete, ready to use computer—not a kit. At $1298, it includes features you won't find on other personal computers costing twice as much.

Features such as video graphics in 15 colors. And a built-in memory capacity of 8K bytes ROM and 4K bytes RAM—with room for lots more. But you don't even need to know a RAM from a ROM to use and enjoy Apple II. It's the first personal computer with a fast version of BASIC—the English-like programming language—permanently built in. That means you can begin running your Apple II the first evening, entering your own instructions and watching them work, even if you've had no previous computer experience.

The familiar typewriter-style keyboard makes communication easy. And your programs and data can be stored on (and retrieved from) audio cassettes, using the built-in cassette interface, so you can swap with other Apple II users. This and other peripherals—optional equipment on most personal computers, at hundreds of dollars extra cost—are *built into* Apple II. And it's designed to keep up with changing technology, to expand easily whenever you need it to.

As an educational tool, Apple II is a sound investment. You can program it to tutor your children in most any subject, such as spelling, history or math. But the biggest benefit—no matter *how* you use Apple II—is that you and your family increase your familiarity with the computer itself. The more you experiment with it, the more you discover about its potential.



Start by playing PONG. Then invent your own games using the input keyboard, game paddles and built-in speaker. As you experiment you'll acquire new programming skills which will open up new ways to use your Apple II. You'll learn to "paint" dazzling color displays using the unique color graphics commands in Apple BASIC, and write programs to create beautiful kaleidoscopic designs. As you master Apple BASIC, you'll be able to organize, index and store data on household finances, income tax, recipes, and record collections. You can learn to chart your biorhythms, balance your checking account, even control your home environment. Apple II will go as far as your imagination can take it.

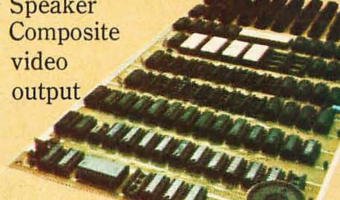
Best of all, Apple II is designed to grow with you. As your skill and experience with computing increase, you may want to add new Apple peripherals. For example, a refined, more sophisticated BASIC language is being developed for advanced scientific and mathematical applications. And in addition to the built-in audio, video and game interfaces, there's room for eight plug-in options such as a prototyping board for experimenting with interfaces to other equipment; a serial board for connecting teletype, printer and other terminals; a parallel interface for communicating with a printer or another computer; an EPROM board for storing programs permanently; and a modem board communications interface, or a floppy disk interface with software and complete operating system. And there are many more options to come, because Apple II was designed from the beginning to accommodate increased power and capability as your requirements change.

If you'd like to see for yourself how easy it is to use and enjoy Apple II, visit your local dealer for a demonstration and a copy of our detailed brochure. Or write Apple Computer Inc., 20863 Stevens Creek Blvd., Cupertino, California 95014.

Apple II™ is a completely self-contained computer system with BASIC in ROM, color graphics, ASCII keyboard, lightweight, efficient switching power supply and molded case. It is supplied with BASIC in ROM, up to 48K bytes of RAM, and with cassette tape, video and game I/O interfaces built-in. Also included are two game paddles and a demonstration cassette.

SPECIFICATIONS

- **Microprocessor:** 6502 (1 MHz).
- **Video Display:** Memory mapped, 5 modes—all Software-selectable:
  - Text—40 characters/line, 24 lines upper case.
  - Color graphics—40h x 48v, 15 colors
  - High-resolution graphics—280h x 192v; black, white, violet, green (16K RAM minimum required)
  - Both graphics modes can be selected to include 4 lines of text at the bottom of the display area.
  - Completely transparent memory access. All color generation done digitally.
- **Memory:** up to 48K bytes on-board RAM (4K supplied)
  - Uses either 4K or new 16K dynamic memory chips
  - Up to 12K ROM (8K supplied)
- **Software**
  - Fast extended Integer BASIC in ROM with color graphics commands
  - Extensive monitor in ROM
- **I/O**
  - 1500 bps cassette interface
  - 8-slot motherboard
  - Apple game I/O connector
  - ASCII keyboard port
  - Speaker
  - Composite video output



Apple II is also available in board-only form for the do-it-yourself hobbyist. Has all of the features of the Apple II system, but does not include case, keyboard, power supply or game paddles. $798.

PONG is a trademark of Atari Inc.

*Apple II plugs into any standard TV using an inexpensive modulator (not supplied).

SEE OUR FULL PAGE DEALER AD ON PAGE 119.



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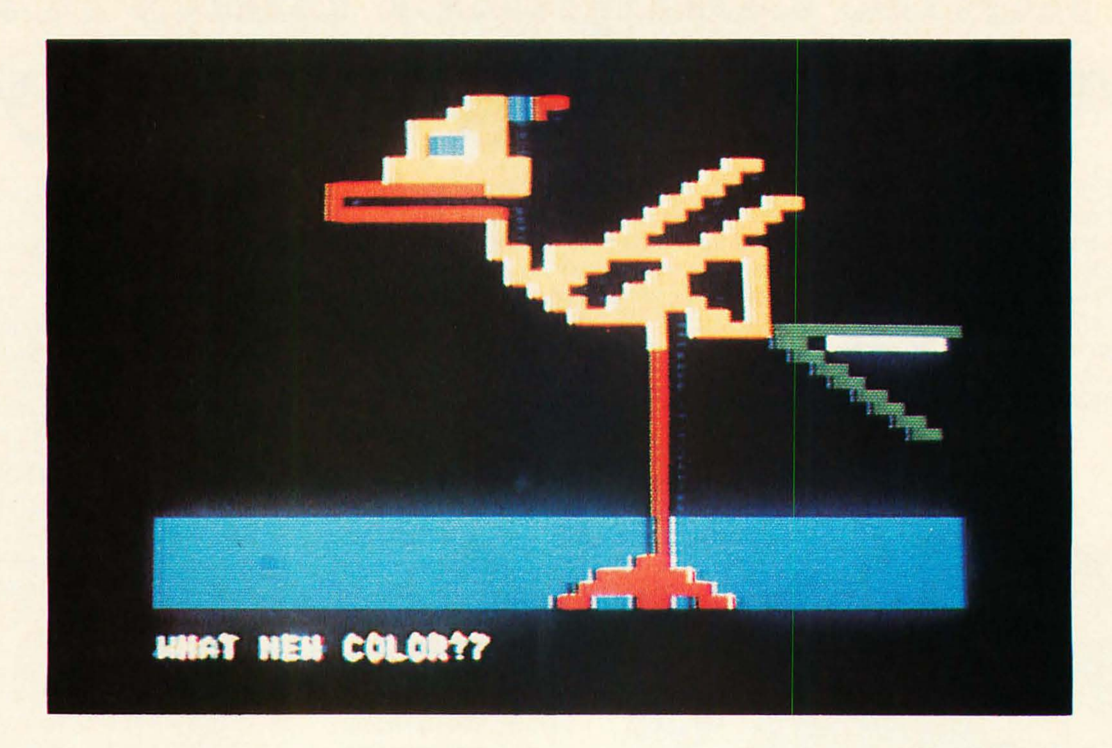


Photo 1: A concoction of color resembling a byrd. This color doodle was produced using a homebrew joystick plugged into the Apple II's game IO connector, and a BASIC program to implement interactive drawing on the television screen. The photograph was made using 1/15th second exposure and ASA 200 Kodachrome slide film in a 35mm camera with macro lens mounted on a tripod. All the color photographs in this article were taken using this setup.

An Apple to Byte

One User's Review of the Apple II

Carl Helmers, Editor

It has been a little over a year since I first became aware of the prototype of the Apple II computer on a visit to Palo Alto CA in November of 1976. At the time I first viewed the Apple II prototype, it was little more than a wire wrapped proof of concept in a homebrew masonite box. In the year since my first exposure to the machine Apple II has become what I consider to be one of the best examples of the concept of the complete "appliance" computer. This variety of computer is sold as a finished product off the shelves of the retailer's shop or by mail from the manufacturer's warehouse. In late October of 1977, I took delivery on an Apple II with 16 K bytes of programmable user memory. After removing it from its shipping box, I connected it to a color television with the cables and radio frequency modulator supplied, and also connected it to an inexpensive tape recorder with an "index" counter to keep track of position. I was able to turn on power and begin using the computer within five minutes of receipt. After one session in my basement laboratory wiring up some joystick hardware using Apple II's documentation as a guide, and after about three evenings of hacking with the built-in ROM BASIC interpreter, I was able to produce a program for a color sketchpad to provide an illustration of some of the potentials of such small computers for use in artistic contexts. While I treat the Apple II as one of the neatest "proofs of concept" of the idea of the personal computer yet to become available, it is by no means the only one on the market, so readers should judge for themselves with respect to their own values and preferences.

The potential for producing graphics like photo 1 illustrates why I became intoxicated with the Apple II concept from the first word of its existence. With a personal interest in the uses of computers for artistic

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FEATURES:

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- Parallel Interface (connector to 3P + S included)
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- Documentation included.
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- High quality Selectric printing.
- Reliable, heavy duty Selectric mechanism.
- Off-line use as typewriter.

$995.

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   Address your request to:
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   ANDERSON JACOBSON, INC.
   521 Charcot Avenue
   San Jose, CA 95131
2. Upon written notification, pick up your terminal at the AJ service office located in one of the above cities. Allow six to eight weeks for delivery.
3. A final check of your unit will be made at the local AJ service office at time of pickup.
4. For warranty or repair service, return unit to designated service location.
5. Available in U.S. only.

CLIP AND MAIL WITH ORDER

Number of units ________ @ $995 each $ ________

Sales tax at delivery location $ ________

Shipping and handling $35 each (excluding San Jose) $ ________

TOTAL $ ________

NAME ________

ADDRESS ________

CITY ________ STATE ________ ZIP ________

PHONE ( ) ________

Circle 4 on inquiry card.



Photo 2: The Apple II in a typical use setting. The television is fairly far away from the computer itself in order to minimize interference and hash generated by the logic circuitry. An inexpensive cassette recorder with turns counter is used to provide mass storage for programs.

purposes, I knew that in principle I should be able to create something like photo 1. Later in this account, I will present the detail design of software which will enable the Apple II user to doodle as I did. I make no claims to great artistic genius, but the ability to do this sort of doodling, as well as much more serious computing in a utilitarian mode of operation, is what the personal computer is all about. Apple II is a self-contained package which talks to a color television set owned by its user, an audio cassette recorder supplied by the user, two control paddles supplied by the manufacturer, and a "kluge harp" style audible annunciator which can be programmed to play music or make a variety of noises. Much of the detail of the system design of the Apple II has already been presented in these pages in the form of an article by its designer, Stephen Wozniak, which appeared in the May 1977 BYTE on page 34. This article will survey the reactions I have had to using this system in the four weeks or so following its arrival.

Externals

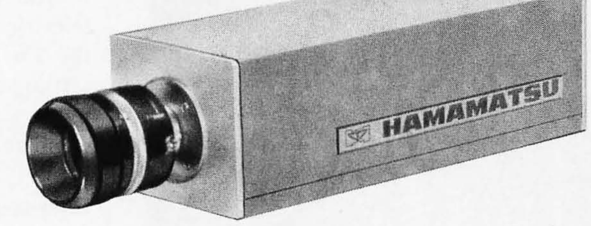
The physical appearance of the Apple II in its normal usage context is illustrated in photo 2. The package in which the system is contained is a high strength injection molded plastic material with a metal bottom plate. The plastic parts are painted an off-white ivory color. The three piece case consists of a body with a door on the top for access to the internal works and peripheral sockets. The case is almost empty when the Apple II arrives, and when carrying the computer around in its optional leatherette bag my common practice has been to take the cover off and insert various paraphernalia cushioned by foam plastic to avoid damaging the circuit boards. (If I had any peripherals plugged into the IO bus of the machine, this would not necessarily be a good idea.) When zipped up in its carrying bag, the Apple II looks like an overgrown pocket calculator. I have taken this computer in its case to friends' homes and with me on trips by airplane (where it fits under the seat as "carry on" luggage). If the destination of one's travels has a color television, and a miniature cassette recorder is packed with the Apple II, then this computer can be considered to be truly portable and adds but one bag to the normal complement of travel luggage.

While the case is elegantly styled, as can be seen from photo 2, there are two minor problems related to the mechanical design of this case. The problems relate to the top of the case and how it fits into the main body of the computer. One problem is the fact that the adhesion between the paint of the case and the plastic is not strong enough to keep the fasteners in place. After I opened the top a few times both fasteners broke loose. The second mechanical design glitch is the fact that if the cover is moved more than about 5 or 10° from horizontal before it is slid out from under the front edge of the case, a leverage effect will tend to extract the keyboard from its moorings.

A usable configuration of the Apple II as emphasized in photo 2 is made up of the computer, a color television, and a cassette recorder. The standard game paddles which come with the system allow interactive graphic applications. The use of a color television is highly recommended, although a black and white set will certainly work, at the expense of one of the unique features of Apple II, its color display.

There are two methods of sending video data to the television set from the Apple. The best option, which is often used by computer stores to show off the system, is use of direct video. However, stock color televisions or color monitors with direct video entry are rare and expensive. A less satisfactory but quite workable method is the use of a radio frequency modulator to generate a television "station" on channel 3, with connection via the antenna terminals and an FCC approved antenna isolation switch which mounts on the back of the set. This method of driving the television is the







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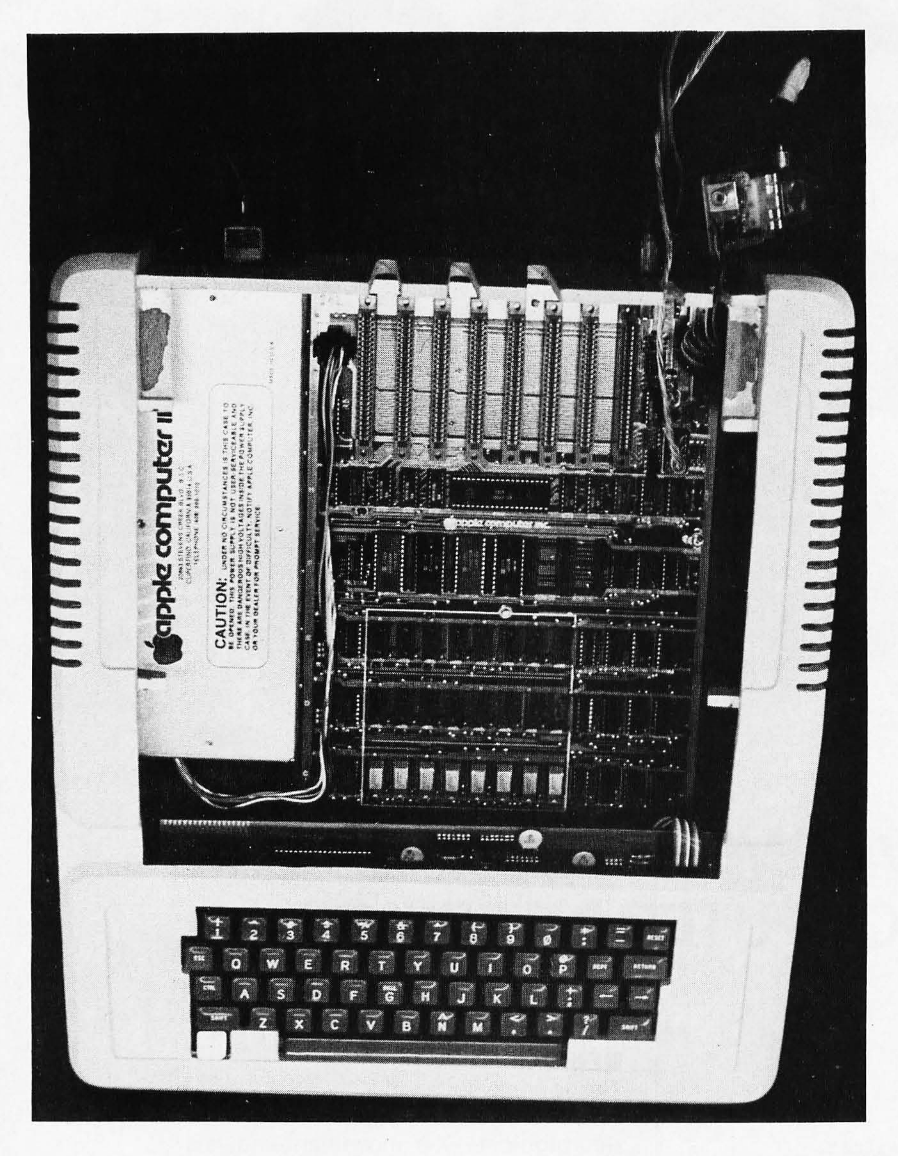


Photo 3: Removing the cover and looking straight down into the unit, the major internal subassemblies can be seen. At the left is the proprietary switching power supply unit; at the right along the bottom of the cabinet is the main processor board, with room for 48 K bytes of programmable user memory (using 16 K memory parts) and an 8 slot IO bus used to interconnect peripherals. At the right toward the rear of the cabinet (top of photo) is the RF modulator used to drive the television on channel 3. The keyboard can be seen toward the lower edge of the photo.

one used in all the photographs and listings accompanying this article.

The main problem with direct RF entry as a method is the tendency of the television set's tuner to pick up RF hash from the digital logic of the computer, a problem which was quite severe in my experience, using a Panasonic color television. The degree of interference is dependent upon the exact positioning of the cable, the television and the computer relative to its various power and peripheral cables. The problem can be minimized, as shown by the fact that in the listings and photos of this article I was able to get a clear picture; but I do not recommend use of a Panasonic television like mine with the Apple II. (Steve Jobs of Apple Computer suggests use of several models of Sony television sets due to superior RF shielding relative to the Panasonic set I used.) If you purchase an Apple II and a color television for it, I highly recommend testing the TV and computer combination prior to settling on a particular television. Some computer stores will convert TV sets to direct video entry, so this provides another option.

Internals

Photo 3 shows the Apple II's interior with the cover removed from the case. The computer is entirely contained on one large printed circuit board on the bottom of the case. At the left is a large metal box containing the switching regulated power supply. The printed circuit board of the keyboard assembly can be seen protruding past the lip at the front edge of the case (bottom of the photograph). Also seen in this picture is a homemade cable running from the game IO connector of the processor board to the joystick box which I built for use with the color sketchpad program to be described. At the top right in this photograph can be seen the RF modulator unit which plugs directly into the main board of the computer. Note that the RF cables contain large toroidal ferrite coil forms with several turns of the cables around them. These are used to minimize (but in my experience with the Panasonic television never totally eliminate) RF hash interference in the television set when the RF modulator technique of video data entry is used.

The Apple II provides a decoded set of eight IO sockets which also feature all the processor bus signals. At the time the Apple II was delivered to me no peripherals were available which used this bus, but I have since seen several advertisements for products to plug into the Apple II bus and the Apple Computer Company is working on peripherals to extend the power of the machine. This bus is completely documented and should work out well for the advanced experimenter.

The Apple hardware includes two fairly gamey peripherals for use in family entertainment situations. One such peripheral is a pair of game IO paddles consisting of an analog input lever and pushbutton switch for each channel. A second such peripheral is the annunciator output which in addition to sounding the "bell" character of ASCII can be programmed by the user with arbitrary pitches, as a sort of music synthesizer.



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The Processor

As documented by its designer Stephen Wozniak in the May 1977 BYTE, the design of the Apple II system uses the 6502 processor created by MOS Technology and now available from several sources. The design has a certain elegance which comes from a simple combination of the video display generation, dynamic memory refresh and processor clock timing based on a single crystal oscillator. I'll not repeat the details here, but simply summarize: the two phase nature of the 6502 clock is such that the processor turns itself off with respect to the outside world during one phase, and accesses memory during the other phase. By using the phase unused by the processor for access of memory by the video display generation logic, there is never any conflict between the display and the processor's access of memory. As a side effect, since the display generator is always cycling through the low order address bits of the dynamic memory content of the machine, the dynamic memory refresh requirements are met by this regular access of memory for display purposes.

The memory address space of the Apple II is partitioned into three major segments. The region from addresses hexadecimal 0 to BFFF (48 K bytes) is reserved for programmable user memory, implemented with dynamic memory parts. The region from D000 hexadecimal to FFFF hexadecimal is reserved for systems software in read only memory, and IO ports are found in the C000 to CFFF region.

The user memory region can have any combination of three 4 K or 16 K byte regions depending upon which memory chips one plugs into three sets of eight sockets. Thus the Apple II can be had with 4 K, 8 K, 12 K, 16 K, 20 K, 24 K, 32 K, 36 K or 48 K bytes of memory at the user's option. For full use of the capabilities of the machine I would not recommend purchasing less than 16 K bytes of memory.

The read only memory regions cover a total of 12 K bytes in the address space, starting at D000 and extending through FFFF. In the versions of Apple II currently being delivered, four 2 K byte read only memory parts are plugged into addresses E000 through FFFF, giving a total of 8 K bytes of systems software and leaving two 2 K byte sockets unused. The present ROM load includes 5 K for the integer BASIC interpreter, 1 K for miscellaneous utility routines, and 2 K for the system monitor program.

Systems Software

As with all the self contained "complete" computer systems, Apple II is ready and willing to act as a personal computer servant as soon as the power is turned on and the "reset" button on the keyboard is pushed. This capability for instant use is achieved by the systems software contained

Continued on page 30

Table 1: Summary of the Apple II 5 K BASIC interpreter.

Variables: Names may be from 1 to 100 characters in length. Data type is numeric unless name is followed by the character "$".

Numeric Variables: May be arrayed up to the limits of available memory with DIM statement. Precision is 16 bits, signed two's complement representation with range −32768 to +32767.

String Variables: DIM statement sets length other than default, from 1 to 255 characters per string.

Speed: Executes the loop 100 FOR I=1 TO 10000,110 NEXT I in about 14 seconds.

Statements:

CALL	NEXT
DIM	NO DSP
DSP	NO TRACE
END	POKE
FOR ... = ... TO ... STEP ...	POP
GOSUB	PRINT
GOTO	PR#
IF ... THEN ...	REM
INPUT	RETURN
IN#	TAB
LET ... = (LET optional)	TEXT
LIST	TRACE
	VTAB

Graphic Statements:

COLOR=	HLIN
GR	PLOT
	VLIN

Operators:

+	=
−	# or < >
NOT	<
↑ (exponentiate)	>
*	<=
/	>=
MOD	AND
	OR

Functions:

ABS	PEEK
ASC	RND
LEN	SCRN
PDL	SGN

Other features:

Branch addresses in GOSUB and GOTO and CALL can be any arbitrary numeric expression which results in a positive value. Legal line numbers are the positive integers 1 to 32767.

Documentation includes several PEEK and POKE strategies to access hardware such as speaker, paddle pushbutton switch inputs, etc.

Other Features: Interpreter Control

AUTO	LOAD
CLR	LOMEM
CON (or control C)	MAN
DEL	NEW
DSP	NO DSP
HIMEM	NO TRACE
GOTO	RUN
GR	SAVE
LIST	TEXT
	TRACE



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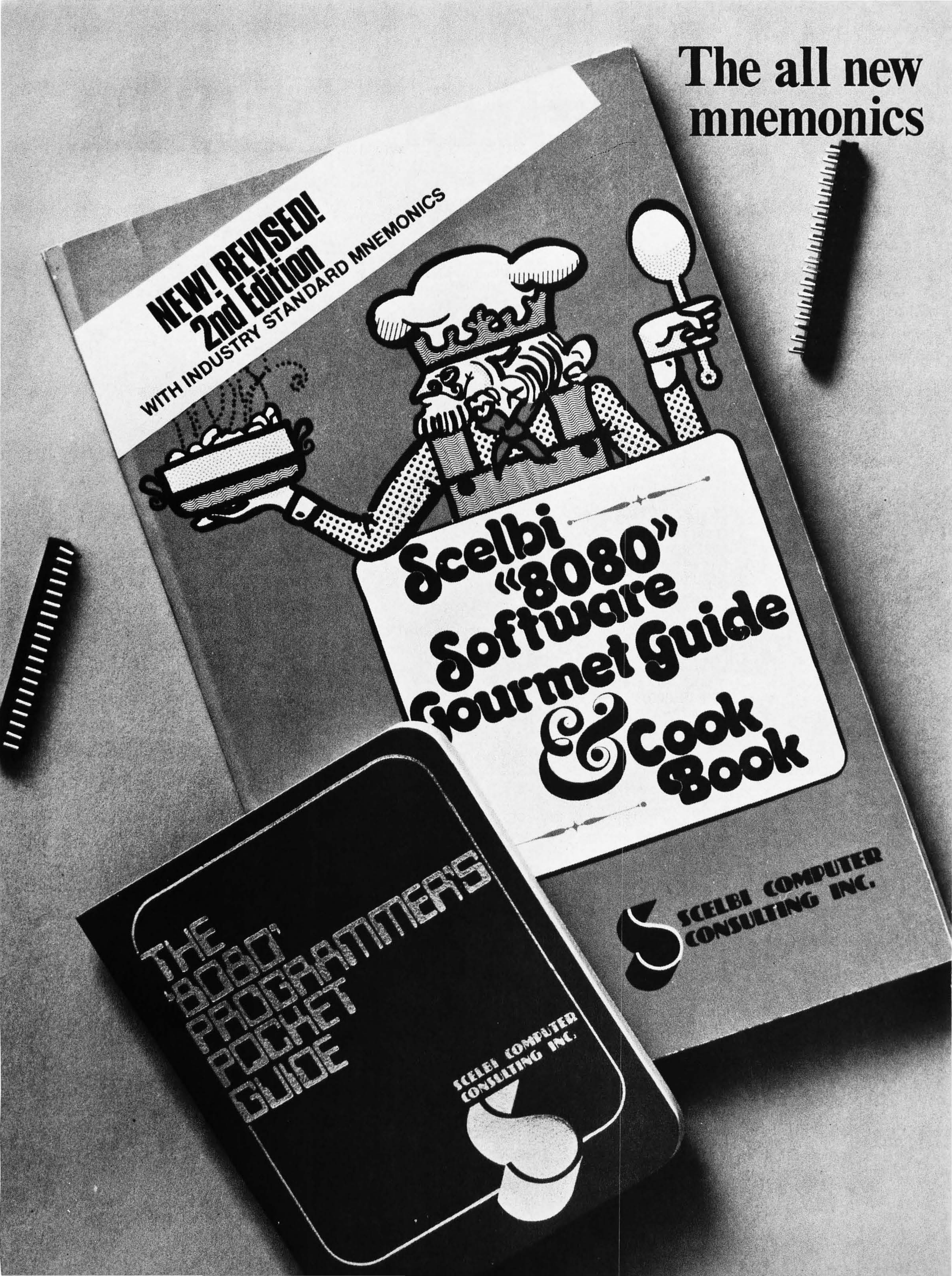
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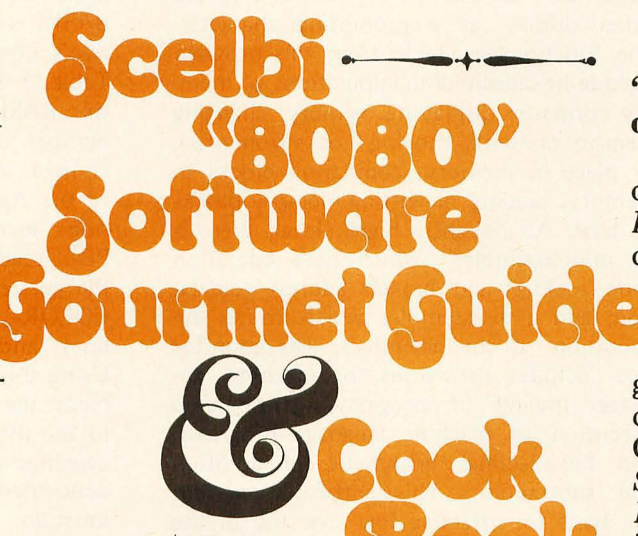
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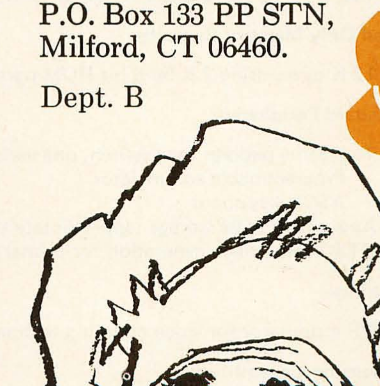
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Continued from page 24

in the 8 K byte read only memory. On reset, the system monitor program is entered, with an asterisk (*) returned to the video display as a prompting character. The functions available from this program include hexadecimal manipulations of memory contents: displaying memory, changing memory contents, moving blocks from place to place in memory, comparing blocks in memory, reading or writing memory blocks to tape. At a slightly higher level, there is a "mini-assembler" which does operation code lookup and branch address calculation, and a disassembler which inverts the operation of the assembler. The monitor also includes provisions for machine language tracing of programs, single step execution of machine language programs, and hexadecimal arithmetic of addition and subtraction. This software provides the basis for effective low level use of the 6502 processor, and in fact was used by Apple II's designer Stephen Wozniak as one of the key software development tools in implementation of the 5 K Apple BASIC interpreter which makes up the remainder of the 8 K software in read only memory.

The 5 K Apple BASIC interpreter is entered from the system monitor through use of a "control B" command followed by a carriage return. This sequence results in the 5 K BASIC interpreter's prompt of an angle bracket (>). The 5 K interpreter built into the Apple II is an integer BASIC with 16 bit precision and a signed two's complement number representation. Table 1 summarizes the characteristics of this BASIC. Built into the language are a number of extensions which are used to control special hardware and the graphics of the Apple II color display. These extensions include the commands GR, TEXT, PDL (read a control paddle), SCRN (extract the current color of a point on the screen), COLOR=, PLOT, VLIN (draw vertical line) and HLIN (draw horizontal line). Using this 5 K BASIC I was able to implement the color sketchpad program shown in the listings of this article, in about three evenings of experimentation which mostly concerned defining just what the program must do.

The 5 K BASIC interpreter which is built into the Apple is all that is needed for implementation of most types of interactive games involving color graphics and reaction times on the part of the user. But the 5 K BASIC, even given its string capabilities, is not what one would want to use to do a simulation of a physical system or calculate quantities other than integers.

As an answer to the need for an extended BASIC as a language for the Apple II, there is the "Applesoft" extended BASIC interpreter which can be used in systems with 16 K bytes of memory or more. The name "Applesoft" is a cross between the source of the interpreter, the Microsoft company, and a gross pun ("applesauce"). This interpreter is nearly identical to the Microsoft extended BASIC interpreters which have been made available for a number of personal computer products. The people at Apple have hacked the interpreter to include a few variations on the standard version which address the color display hardware. The only relative novelty of this hack is that in order to get graphics extensions, they had to sacrifice two statements: LET and REM. Thus, on initialization of Applesoft, the user is given the option of having LET and REM but no built-in graphics primitives, or having graphics but no LET and REM statements. Since LET is totally optional in assignments, its loss is hardly felt; but the lack of remarks may be felt by self-documenting code purists who want to use the graphics mode of Applesoft. Of course not having the primitives does not prevent use of the graphics hardware, since like all Microsoft interpreters, Applesoft has PEEK and POKE

Table 2: Summary of Apple II features.

Processor: 6502 running at 1.023 MHz

User Memory Capacity: Three banks of eight 4 K or 16 K dynamic memory parts
4 K, 8 K, 12 K, 16 K, 20 K, 24 K, 32 K, 36 K or 48 K bytes

Read Only Memory Capacity:

12 K bytes using 2 K by 8 bit ROM parts, 8 K installed

Standard Peripherals:

Two game paddles (one switch, one variable analog input per paddle)
Programmable annunciator
ASCII keyboard
Audio tape mass storage (approximately 1500 bps)
NTSC color video generation for primary display

Optional:

RF modulator for video coupling to standard television

Expansion Capabilities:

Eight IO connectors with 50 pins:
Full address bus (16 pins)
Full data bus (8 pins)
Timing signals
DMA signals
Device select signals

Software:

System monitor (2 K bytes, ROM)
Utility routines (1 K bytes, ROM)
Integer BASIC interpreter (5 K bytes, ROM)
Full extended BASIC (Applesoft, loaded from tape, requires 16 K user memory)
Applications software examples including games, accounting, etc

FOUR STAR PERFORMERS FOR THE S-100 BUS

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THE NORTH STAR S-100 FAMILY—four high performance products at attractive low prices. Our boards are designed for use in the North Star HORIZON computer and other S-100 bus computers using 8080 or Z80 processors. Visit your computer store for a demonstration, or write for our free color catalog.

16K RAM BOARD

No other S-100 bus memory can match the performance of the North Star 16K RAM at any price. This low-power board has been designed to work at full speed (no wait states), even at 4MHz with both Z80 and 8080 systems. Memory refresh is invisible to the processor, bank switching is provided and addressability is switch selectable in two 8K sections. Best of all, a parity check option is available. Kit: $399. Assembled: $459. Parity Option — kit: $39. Assembled: $59.

MICRO DISK SYSTEM

The North Star MDS is a complete floppy disk system with *all* hardware and software needed to add floppy disk memory and a powerful disk BASIC to S-100 bus computers. The North Star MDS is widely considered one of the best designed and most complete S-100 bus products available. The MDS includes the S-100 interface board with on-board PROM for system startup, Shugart mini-floppy disk drive, cabling and connectors, and DOS and BASIC software on diskette. Kit: $699. Assembled: $799. Additional drive — Kit: $400. Assembled: $450. Single Drive Cabinet: $39. Optional Power Supply: $39.

Z80A PROCESSOR BOARD

The North Star ZPB brings the full speed, 4MHz Z80A microprocessor to the S-100 bus. Execution is more than twice the speed of an 8080, and the ZPB operates in systems both with and without front panels. The ZPB includes vectored interrupts, auto-jump startup, and space for 1K of on-board EPROM. Kit: $199. Assembled: $259. EPROM Option — kit: $49. Assembled: $69.

HARDWARE FLOATING POINT BOARD

If you do number crunching, then this board is for you. The FPB performs high-speed floating point add, subtract, multiply and divide with selectable precision up to 14 decimal digits. Arithmetic is up to 50 times faster than 8080 software, and BASIC programs can execute up to 10 times faster. A version of North Star BASIC is included. Kit: $259. Assembled: $359. Prices subject to change.

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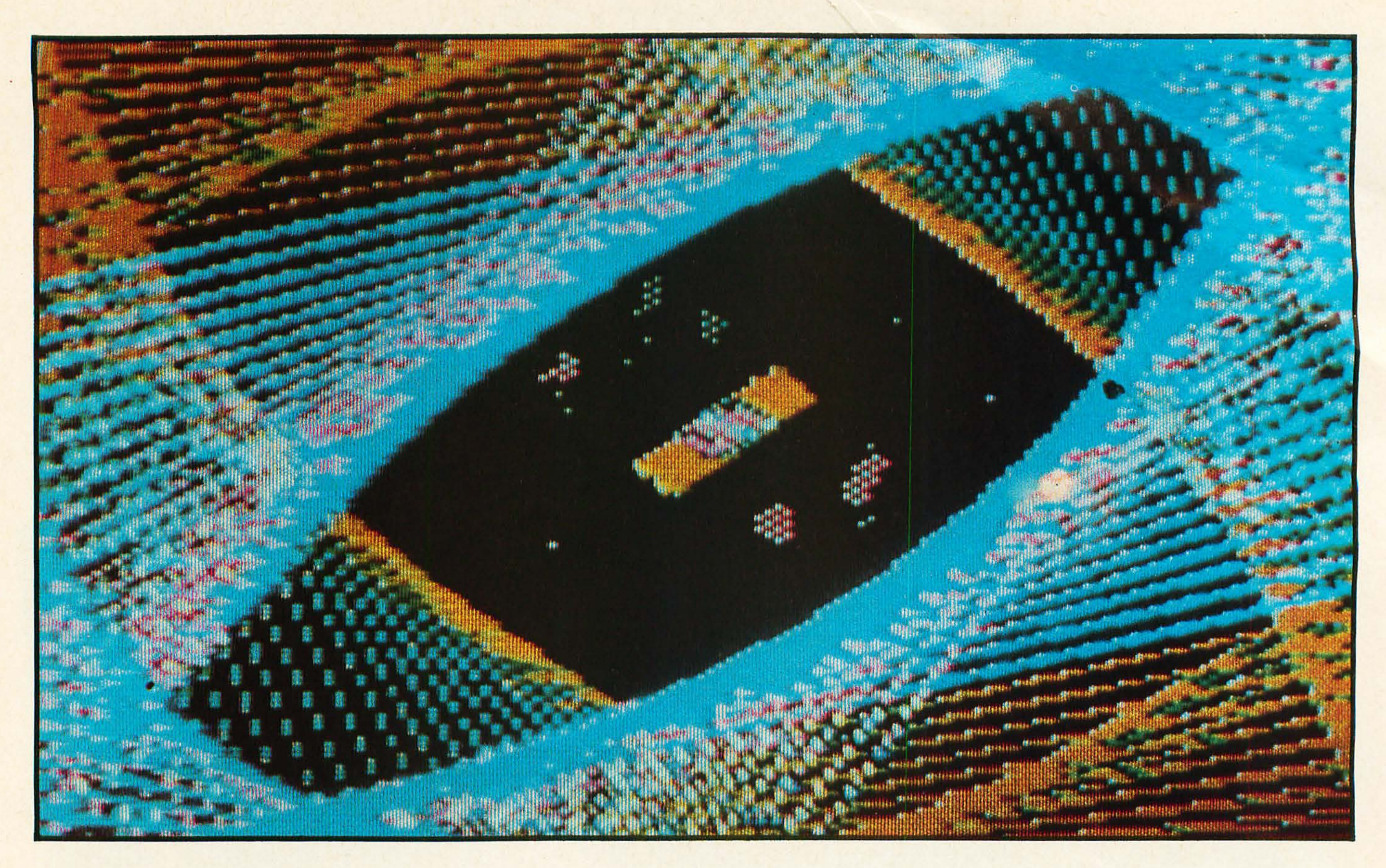


Photo 4: An example of the high resolution graphics hardware of the Apple II is provided by this photo. Although four nominal colors are available, this photo illustrates how some subtleties of color can be obtained by taking advantage of the distortions inherent in the television set when manipulating controls. This demonstration is one of several options available in the high resolution graphics demonstration program of Apple II.

primitives and all hardware addresses are documented in the Apple II.

The Applesoft interpreter is loaded from its cassette tape using the LOAD command of the 5 K interpreter. It takes about one minute and 30 seconds to do this load, which results in what 5 K BASIC thinks is a really big application program, but what is in effect the object text of the new interpreter plus a 5 K BASIC program which presents an interactive setup sequence. After loading this pseudo 5 K BASIC text, the user types RUN, and the interactive setup sequence is entered. This sequence includes the option to display a summary of Applesoft BASIC commands which is also available on a reference card. After the setup sequence, the Applesoft interpreter is entered, as indicated by a right square bracket prompt character (]). With a 16 K Apple II system, the user gets the message "5615 BYTES FREE" at the conclusion of the setup sequence.

Running the same rather incomplete benchmark as is found in table 1, I found that the Applesoft interpreter running in an Apple II took 12 seconds for 10000 iterations of a null loop.

Tape Mass Storage

The Apple II tape mass storage system accomplishes its purposes of storing and recovering files of data. I have proven this to my own satisfaction by using the system. For both the 5 K BASIC and Applesoft BASIC, SAVE and LOAD operations feature a "beep" from the Apple II's annunciator following the leader at the beginning of the file, and at the end of the operation. There is no such audible feedback when using the tape with system monitor commands.

It is the user's responsibility with the Apple II tape system to keep track of files on a piece of paper or in a log book. The software of the tape system does not include any naming of files in file headers. It also does not include any "verify" command for those of us who would like to make sure that a file is properly written before pulling the plug and closing down at the end of an evening's programming.

The act of loading a file involves the user positioning the tape just past the start of the leader tone for the file, issuing the proper command up to the point of the carriage return which completes the command line, then simultaneously starting the recorder and hitting the carriage return key.

High Resolution Graphics Software?

The one item of systems software which has been promised but not yet (December

Continued on page 35

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Circle 100 on inquiry card.

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Next, we picked a male/female connector. Not only is it less expensive than edge connectors, our tests show it's also more reliable! And because it costs less, every H8 motherboard includes all the connectors you need for expansion. There's nothing extra to buy.

The connectors are mounted on the right side of the cabinet at an angle so the boards tilt back. That gives us a couple of significant advantages. First, it allows the boards to be larger without requiring a taller cabinet. So our circuit board layout is more open, which makes the boards easier to build – even if you've never built a kit before. Second, the angled mounting provides easy accessibility to all the components on the face of the boards without an extender. (Many times an extender alters the transmission characteristics of the bus, which masks the problem you're trying to solve or even causes new ones.)

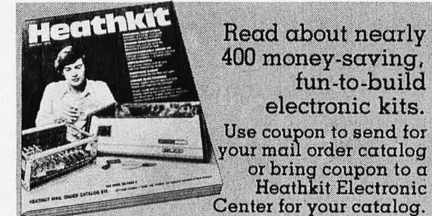
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Continued from page 32

1977) delivered to me in a documented form is the "high resolution" graphics software package. This is perhaps the best attribute of the Apple II's unique color graphics orientation; its potential is shown by a "high resolution demo" program which I was able to get from the company, including a number of graphic whizbangs selected from a list of choices. Perhaps the best in my opinion is something called the "Spirograph," a constantly changing color graphic implementation of a mandala. The illustration of photo 4 is taken from one state of this program's execution approximately six hours into its evolution one evening. The program uses a random number generator which appears truly random (unrepeatable upon reloading from the same tape) to control the course of the pattern. The price of the graphics routines is listed as $10.

Applications Software

A mixed bag of user oriented software is available with Apple as a means of demonstrating the system. This includes a number of tapes with games using the display and paddles, a "Checkbook-Home Management" package, an excellent 16 K Star Trek game which I have used on my system several times, etc. Typical prices are around $10 per tape, with four tapes currently listed in the catalog sheet. Users can expect more offerings as time goes on. It is these applications programs, games and graphic whizbangs, which provide the greatest value to me when demonstrating the concept of a personal computer to friends.

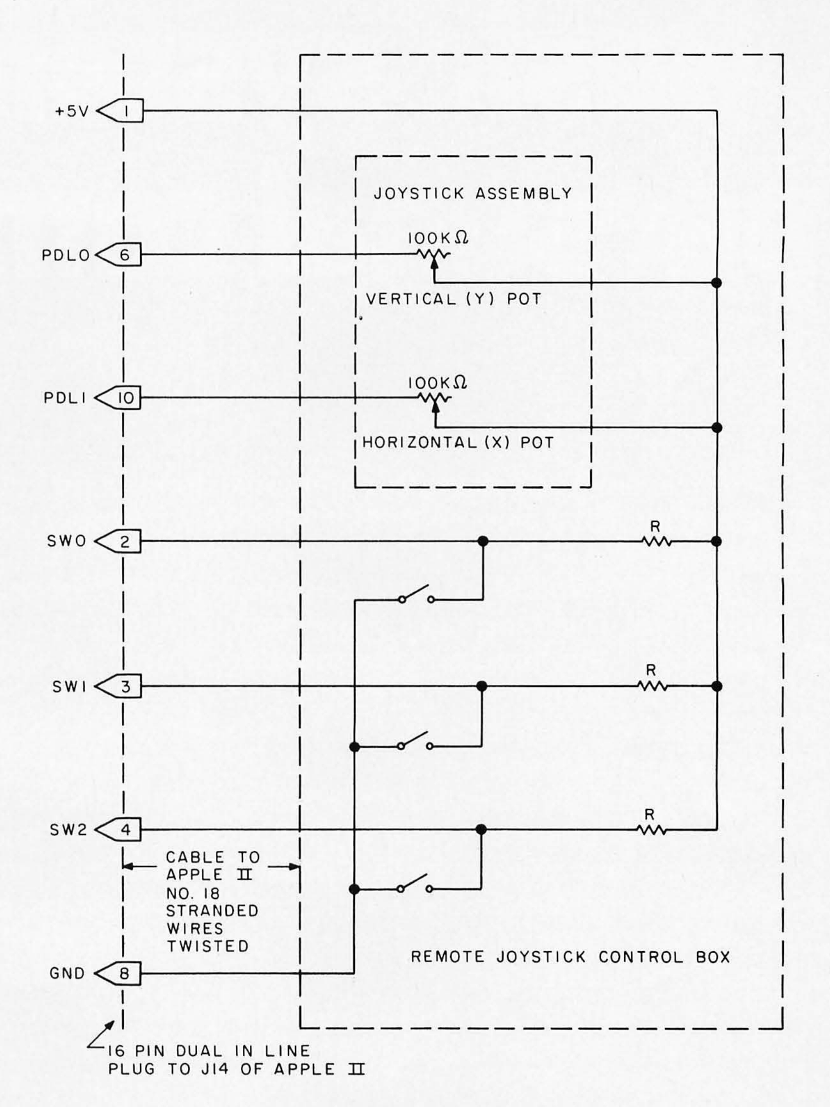


Figure 1: Wiring of the joystick control box and cable. The box is shown in photo 5. The cable used was made up of separate #18 stranded wires, twisted after all interconnection to the plug had been completed.

Documentation

Aside from having a well designed hardware configuration, the Apple II is not hidden from the user who wants to figure out what is in his computer. The "preliminary" documentation which I have on the Apple II consists of a loose leaf file bound in a report folder which has proved anything but preliminary in terms of completeness and usefulness. Its contents are not excessively verbose, but all the essentials are present: the specification of the syntax of the 5 K BASIC, how to access systems software hooks from BASIC, the complete address space map of the hardware, and neat comprehensive drawings of all of the system's electronics. When it came time for me to wire up a version of the game paddles in the form of my own joystick hack, I was able to turn to a page of the manual containing a specification of all the signals on the 16 pin game IO connector. This manual is not a tutorial on how the computer works, but it does contain all the information needed for the experienced experimenter to add custom hardware to the system. A "final" version of the manual is in preparation according to the Apple Computer Co, but this preliminary manual is complete enough to stand on its own.

The only items where I found documentation somewhat scanty were the Applesoft BASIC interpreter (documentation limited to a reference card quoting the initialization texts on how to use it), and the lack of documentation of high resolution graphics to date.

Using the Apple II: A Color Sketchpad Program and Joystick

As a means of trying out the Apple II system and its documentation, I set a goal of

Continued on page 40

Basic systems for personal computing

If you are just getting into personal computing and are looking for a starter system, you have two choices: a computer kit with RAM memory only or a fully assembled computer with BASIC-in-ROM. From reading this magazine and talking to computer buffs it should be obvious that it is desirable to have a computer capable of communicating in the programming language BASIC. This language allows you to instruct the computer in English-like phrases and to use any of the thousands of standard programs written in BASIC (there are probably several in this magazine).

If you purchase a (RAM-only) computer kit you will have to buy additional RAM (4K to 8K), a terminal, and cassette interface for a total cost of about $1000 to run BASIC after you get the kit together and working. Your reward for this endeavor will be a wait of about 15 minutes every time you turn the computer on just to load BASIC into the machine!

Your other alternative is a BASIC-in-ROM computer. These machines have BASIC built in so that it is there whenever the computer is turned on. BASIC-in-ROM computers are also usually fully assembled and cost far less than the RAM-only kits because they are mass-produced by the thousands.

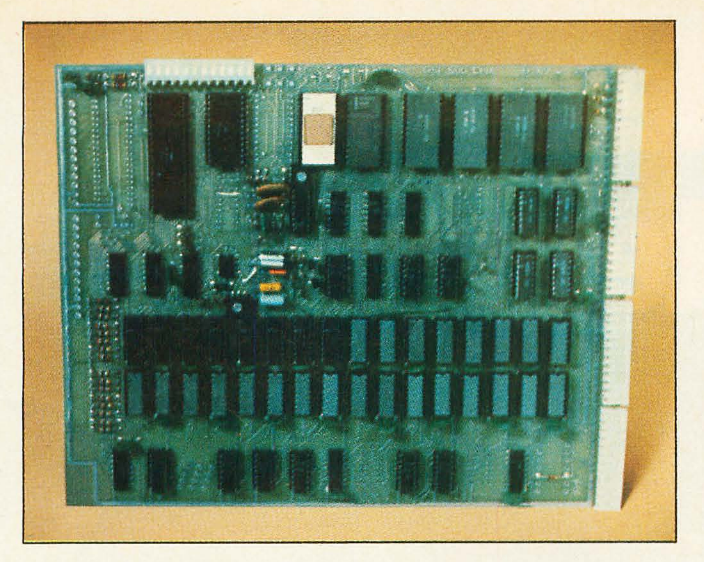
But, you must be careful when selecting a BASIC-in-ROM computer. Some models do not have full-feature BASIC. Instead they have Tiny BASIC or 4K BASIC which cannot run most of the standard BASIC programs available. Still others have other shortcomings such as a small calculator-style keyboard which makes program entry difficult, or most important, lack of expansion capability, preventing the computer from growing with you.

Ohio Scientific offers you a line of expandable computers with full-feature 8K BASIC-in-ROM. They all come fully assembled and tested, but give you the option of economizing by supplying the simple things — power supply, keyboard and TV, if desired, so that you get the most computer power for your dollar.

Compare Ohio Scientific's $298 BASIC-in-ROM Model 500 Board (1MHz clock), which has our Version 3.3 BASIC, against other small computers, as in the independent article "BASIC Timing Comparisons" (Kilobaud, Oct. 1977, p. 23). In this test, the Model 500 excelled over all our personal computing competitors, and was second in performance only to our Challenger disk systems, compared against twenty-eight other computer systems. And the Model 500 is our lowest-cost machine! Our larger models are even more dramatic in a comparison with any competitive models.

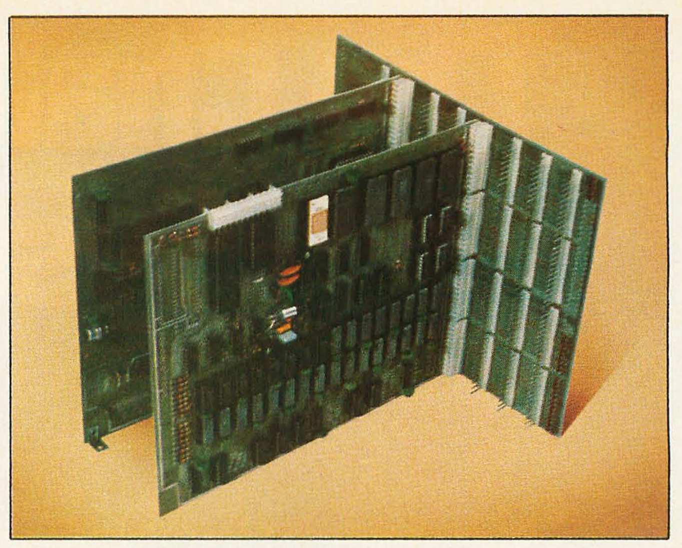
Having the fastest full-feature BASIC ROMs certainly isn't the only criterion necessary for a superior computer system, but it sure helps. Ohio Scientific offers all the other features necessary, including a full line of computer accessories complete with 15 accessory boards available in over 40 configurations. Many Ohio Scientific accessories are so innovative that no one else in the industry has them — such as dual port memory boards, multi-processing CPU's and big disks.

Ohio Scientific has other unique features for the personal computerist. For instance, there is Ohio Scientific's *Small Systems Journal*, published bi-monthly, a full magazine aimed specifically at the owners of Ohio Scientific computers. If you are looking for a personal computer, be sure to look carefully at Ohio Scientific. We think you will find that we have the system for you.



Model 500 Board

A full 8K BASIC-in-ROM computer on a board. This unit contains a 6502 microprocessor with our powerful 8K BASIC-in-ROM, 4K of RAM memory, and a serial port which can be jumpered for 20ma current loop or RS-232. The board can be plugged into any standard OSI-backplane and expanded by our full line of accessory boards. The user must simply supply +5V and −9V power and the serial terminal to be up and running in BASIC. **$298.00**



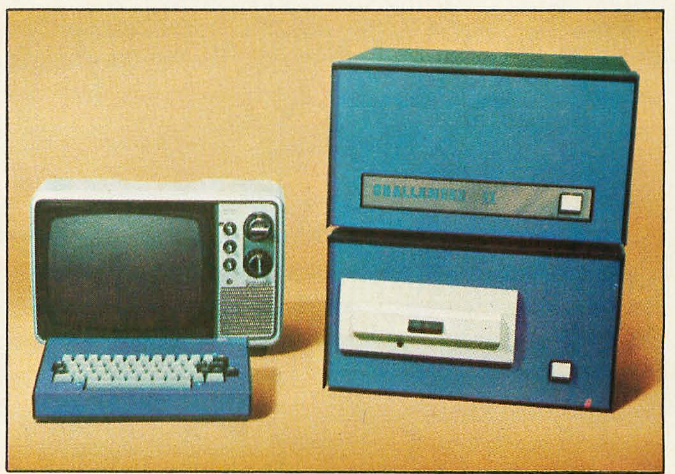
Super Kit

An ideal starter computer system. The Super Kit includes a Model 500 CPU Board with 8K BASIC in ROM, CPU, and 4K of RAM, full buffering for expansion, an eight-slot backplane board, and a Model 440 Video I/O Board. Model 440 provides full CRT functions when connected to a video monitor or modified television set and a standard ASCII keyboard. The user must simply provide +5V and −9V power, an ASCII keyboard, and a modified television set or monitor to have a full computer system with 8K BASIC-in-ROM, 4K user space and a CRT terminal with scrolling. **$398.00**



Challenger II·P

Our very popular fully packaged BASIC-in-ROM computer. Challenger IIP contains the Model 500 CPU Board with 4K of RAM, our new 540 32x64 character video display, keyboard and complete audio cassette interface. The unit also has internal power supplies and a four-slot backplane with two open slots for expansion. The user has only to connect a monitor or modified television set to its output, and he is ready to program in BASIC. To store programs and data files, he needs only to connect a conventional audio cassette recorder to the built-in audio cassette interface. The unit is fully assembled and ready to go. **$598.00**



Challenger II Disk Systems

The ultimate in personal computing offered by Ohio Scientific is the Challenger II system with single- or dual-drive full-sized floppy disk. Each floppy stores 250,000 characters. The Challenger II is available as a video system with keyboard so that all the user needs is a television or monitor for operation; or as a serial version where the user must supply his own terminal. Challenger II disk systems automatically load in BASIC and now have an extensive library of high-performance programs. The programs are ideal for the advanced hobbyist, educational users, industrial development and small business applications. Challenger II disk systems are very economical. For instance, a 16K disk system with 250,000 bytes of disk storage starts at under **$2000.00**



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For more information contact an Ohio Scientific dealer or send $1 for our 64-page buyers' guide.

The Challenger III System

When considering cost effective computers for small business applications, the prospective buyer really has only a few choices: Ohio Scientific's factory-assembled fully integrated computer systems, or the multitude of "pot-luck" 100 systems.

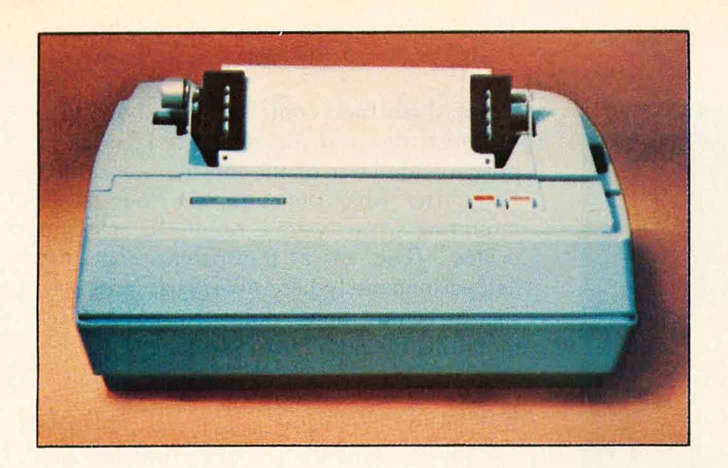
First consider the 100 system. It is a computer system defined as a collection of S-100 components. It is offered by computer stores and systems houses who mix CPU boards, memory boards, cases, mini-floppies, full-size floppies and numerous software packages from many different vendors. In many cases the components even vary from system to system. Unfortunately, what is often used in a computer system is simply what the computer dealer has on hand at the moment. This may include off-brand or obsolete boards, among other things.

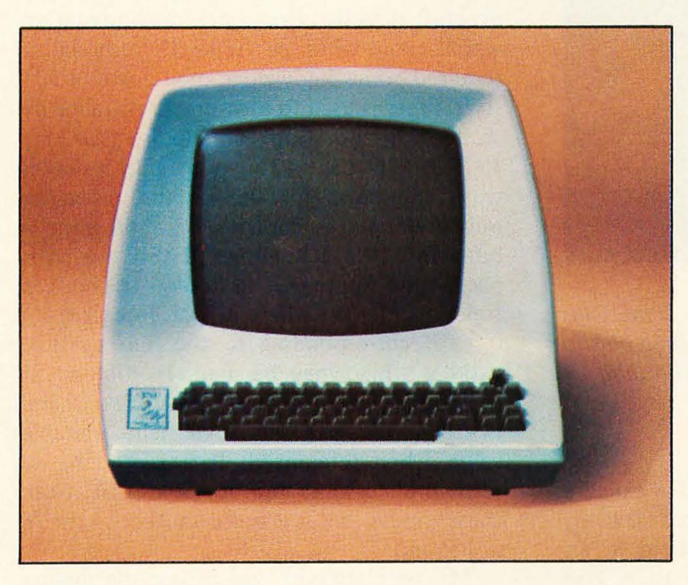
The end user of these pot-luck 100 systems may experience dissatisfaction with the system. First of all, all S-100 products are NOT compatible with each other, as is commonly assumed. The same is true for hardware products, and most certainly for software products. So although the user may be able to get one or more software packages from the dealer along with the computer system, it can be a battle from there on converting software to run on his computer.

The second problem is service. If the customer moves or the dealer goes out of business, the customer is out of luck because virtually no one will service computer systems of mixed origin. The computer system might even have been built from kits since most S-100 manufacturers offer their products in kit form. Several charge outrageous prices for assembled products. And then there is future expansion — this can be difficult because all S-100 products are not created equal or compatible!

We could go on with this horror story, but let us take a more positive approach and look at the other alternative — the factory-integrated computer system. Ohio Scientific manufactures a full line of computers and accessories which are not compatible with S-100 equipment, but are fully compatible with our full line of expansion accessories. All of our systems-level equipment has always been available only in fully assembled form. When you buy an OSI small business system from a dealer, you are assured of buying a standard computer system that was factory assembled and tested. You can be assured of getting service from any of Ohio Scientific's dealers and direct from the factory, now and in the future, whether you stay in your present location or move across the country.

A standardized system means standard software. You can order any of Ohio Scientific's library of diskettes, put them in your disk drive, and your system will perform immediately. And you can make use of our large dealer-generated software library which runs on all Ohio Scientific disk systems. Finally, regardless of the possible pitfalls with other computer systems, Ohio Scientific's Challenger II and Challenger III business systems stand on their own, based on ultra-high performance and impressive performance/cost ratio. Look carefully at the specifications of the Challenger III system on the following page. Compare the advantages of a factory-integrated and supported computer system with those of a computer system of mixed origin. We think you will agree Ohio Scientific is the only sensible choice in cost-effective small business computing.







- Designed for small business computing.
- Uses the 510 triple processor CPU Board, runs 6502, 6800, 8080 and Z-80 programs.
- Available with up to 1 Megabyte of RAM memory; high reliability static RAM is standard; low-cost dynamic RAM is optional.
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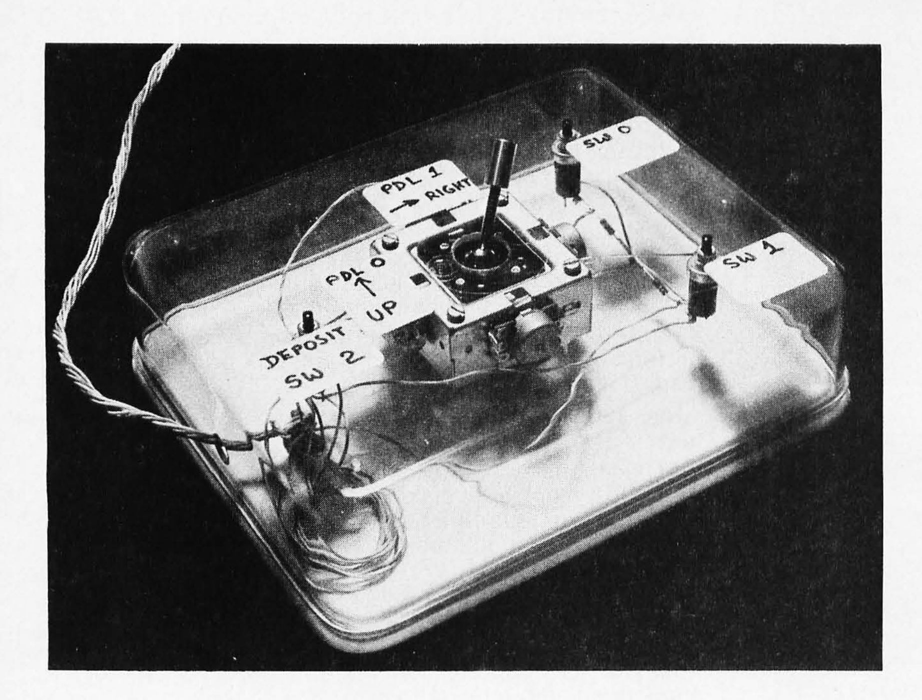


Photo 5: The joystick box which was implemented in order to create the color sketchpad application of listing 1. The cabinet is a gourmet plastic food container obtained at a retail outlet. The box is wired according to figure 1, which was created using the Apple II documentation.

Continued from page 35

implementing a version of what was called a "Cybernetic Crayon" by Thomas Dwyer, Leon Sweer and Margot Critchfield in an article we published in November 1976. The first requirement was that of creating a joystick input to replace the separate control paddles which are standard from the manufacturer of Apple II. Then with the joystick box tested and working, I would create software which would use the joystick and the Apple II keyboard to create color doodles within the 40 by 40 matrix of the television screen in the low resolution graphics mode of operation.

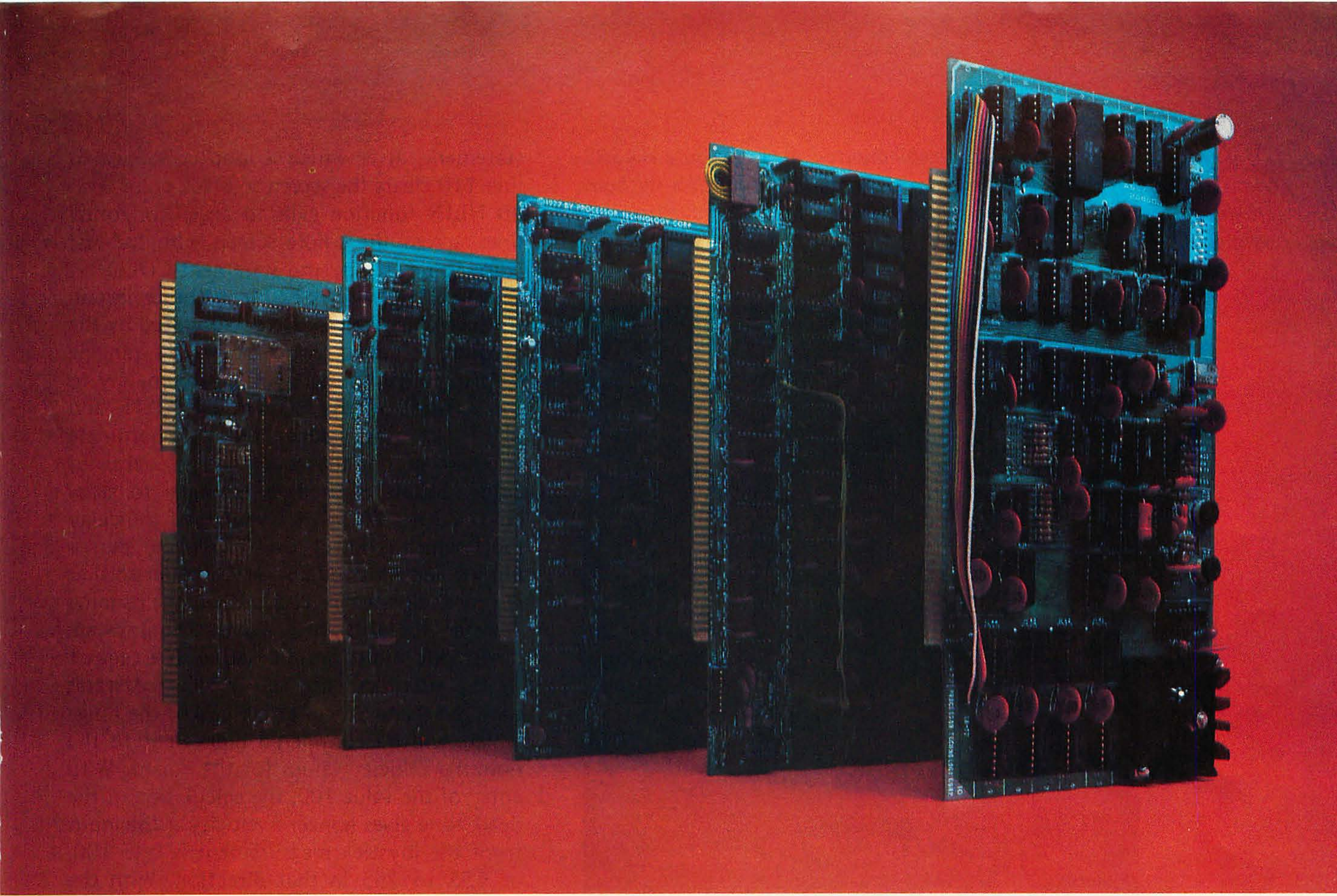
The creation of a joystick box with the Apple II is a simple matter of wiring. The manual lists the complete set of signals available at the game IO connector, a 16 pin dual in line socket located near the rear of the main board of the computer. The wiring is given in figure 1, showing the essentials of two resistance measurements inputs (PDL(0) and PDL(1) in 5 K BASIC) and three switch inputs. The actual box which I created is shown in photo 5. The joystick, which was purchased from James Electronics, has four 100 K potentiometers, of which only two are used, one on each axis. The switches were pushbuttons removed from an archaic surplus digital test jig (circa 1960 technology). The entire device was mounted in the bottom of a gourmet food container which I purchased retail at a shopping mall for this purpose. (I actually had to buy a matched set of three food containers for about $10, of which one was the right size.) The large hole for the lever of the joystick was drilled first, after which holes for the four #4-40 mounting screws were carefully located and drilled. (Use of a transparent container helped immensely here.) Wiring according to figure 1 was done point to point after mounting the push button switches.

Making a Program...

The wiring of the actual control box was derived directly from the documentation which came with the Apple II (although it required some knowledge of the way a 555 style timer is used to measure a resistance by controlling the width of a pulse (see May 1977 BYTE, page 42, figure 2)). In a similar way, the hook for use of the resistance measurements as controls of a program is built into the 5 K integer BASIC which is part of the Apple II. This hook is the built in function PDL(x) where x is an integer from 0 to 3 corresponding to the four possible paddles which may be used. In the case of the paddle box of figure 1, only PDL(0) and PDL(1) will give any externally variable value when referenced. It is one thing to read the cursor value for a display from these inputs, but it is quite another to use it, as I found.

My first attempt was to use the integer value from 0 to 255 returned by PDL(n) as a direct cursor control for the position of an action being performed on the screen. The only problem here was that when I normalized the values to a range of 0 to 39 appropriate for the 40 by 40 matrix of points of the Apple II, the characteristics of my potentiometers prevented fine control of which point on the screen was addressed (certain points proved totally unadddressable). My second attempt was to use a tabular transfer function to convert observed value to a 0 to 39 coordinate value. After this did not work well, as a final expedient I then reduced the joystick inputs to the logical equivalent of a set of four single pole single throw switches which would input an effective "velocity" value of −1, 0 or +1 for each axis of motion of the joystick. Once I had an effective way of input for the cursor motion commands defined by the joystick, I could begin to design a program to allow definition of color values, and depositing of colors under control of one of the switch inputs of the control box.

The final program, a result of several iterations, is given in listing 1, photographically reproduced from the screen of my television display. The program begins with setting of the "graphics" mode with the GR



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Listing 1: The color sketchpad program, implemented in 5 K Apple BASIC. Showing complete lack of form, this program is written by its author without REM statements to explain what is going on. See the text of the article for detailed comments.

```
   5 DIM T$(100)
 100 GR : COLOR=0
 110 FOR I=0 TO 39: HLIN 0,39 AT
     I: NEXT I
 120 X=20:Y=19
 130 ODEP=0:DEPOSIT=0
 140 SCOL=0
 160 LNG=2
 170 BLINK=LNG
 179 PRINT "WHAT ARE JOYSTICK "
 180 INPUT "DEAD ZONE LIMITS=",DZ
 190 ZD=255-DZ
1000 KEY= PEEK (-16384)
1003 GOSUB 8700
1005 GOSUB 3000
1010 IF KEY<128 THEN GOTO 1000
1015 POKE -16368,0
1030 IF KEY= ASC("F") THEN 2000
1051 IF KEY= ASC("Q") THEN 8000
1052 IF KEY= ASC("C") THEN 8500
1053 IF KEY= ASC("T") THEN 2500
1054 IF KEY= ASC("J") THEN 179
1070 GOTO 1000
2000 PRINT : PRINT : PRINT
2010 INPUT "FILL SCREEN WITH COLOR="
     ,CC
2020 IF CC<0 OR CC>15 THEN 1000
2030 COLOR=CC
2040 FOR I=0 TO 39
2050 HLIN 0,39 AT I: NEXT I
2055 SCOL=CC
2057 GOSUB 2600
2060 GOTO 1000
2500 PRINT : PRINT : PRINT
2510 PRINT "ENTER TEXT TAG FOR DRAWIN
     GS"
2520 INPUT T$
2530 GOSUB 2600
2540 GOTO 1000
2600 PRINT : PRINT : PRINT : PRINT
     T$
2610 RETURN
3000 BLINK=BLINK-1
3010 IF BLINK=0 THEN 3100
3020 IF BLINK=LNG/2 THEN 3200
3030 RETURN
3100 COLOR=0
3105 IF SCOL=0 THEN COLOR=6
3110 PLOT Y,X
3120 BLINK=LNG
3125 GOTO 3300
3200 COLOR=SCOL
3210 PLOT Y,X
3220 RETURN
3300 XX= PDL (0):YY= PDL (1)
3310 IF XX<DZ THEN GOSUB 6000
3320 IF YY<DZ THEN GOSUB 7000
3330 IF XX>ZD THEN GOSUB 6500
3340 IF YY>ZD THEN GOSUB 7500
3350 RETURN
6000 COLOR=SCOL: PLOT Y,X:X=X-1
6010 GOTO 9900
6500 COLOR=SCOL: PLOT Y,X:X=X+1
6510 GOTO 9900
7000 COLOR=SCOL: PLOT Y,X:Y=Y-1
7010 GOTO 9900
7500 COLOR=SCOL: PLOT Y,X:Y=Y+1
7510 GOTO 9900
8500 PRINT : PRINT : PRINT : INPUT
     "WHAT NEW COLOR",SCOL
8510 SCOL=SCOL MOD 16
8519 GOSUB 2600
8530 GOTO 1000
8700 DEPOSIT= PEEK (-16285)
8710 IF DEPOSIT<128 THEN 8740
8720 DEPOSIT=-1
8730 GOTO 8750
8740 DEPOSIT=0
8750 IF DEPOSIT=ODEP THEN RETURN

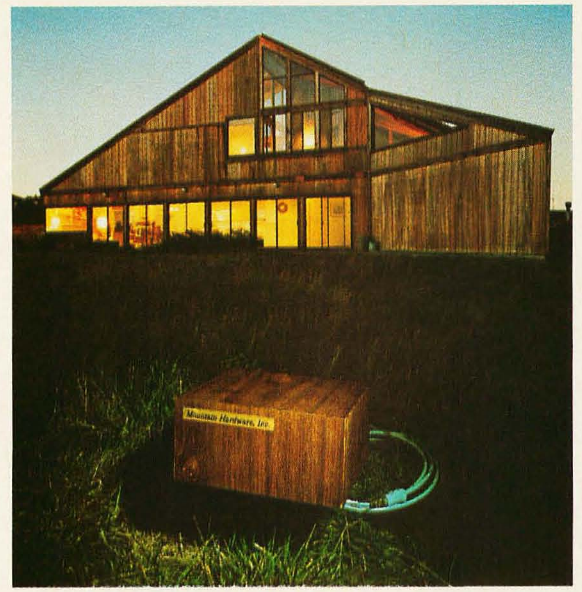
8760 IF DEPOSIT=0 THEN 8800
8770 QQ=SCOL
8780 ODEP=DEPOSIT
8790 RETURN
8800 SCOL=QQ
8810 ODEP=DEPOSIT
8820 RETURN
9900 IF X<0 THEN X=0
9902 IF X>39 THEN X=39
9904 IF Y<0 THEN Y=0
9906 IF Y>39 THEN Y=39
9908 IF DEPOSIT THEN 9950
9910 SCOL= SCRN(Y,X):BLNK=LNG
9920 RETURN
9950 COLOR=SCOL
9960 PLOT Y,X
9999 RETURN
```

statement, after which a loop contained in line 110 clears the screen to black color with 40 HLIN function calls to draw horizontal lines across the whole screen with the last color value (set by the statement COLOR = 0 in line 100). Lines 120 to 190 then initialize several variables. X and Y are used by the program as the current cursor values, ranging from 0 to 39, initially set approximately to the center of the screen. DEPOSIT and ODEP are flag values used to coordinate whether or not the cursor leaves a trail of color. SCOL is used temporarily to store color values. LNG is the length of the delay loop which controls how fast the cursor blinks, and must be an even number so that it can be divided by 2. BLINK is the running counter for this delay loop. The joystick dead zone limits are defined with a request to the user, and are the number of states between 0 and 255 at either end of the range which will be considered equivalent to the nonzero velocity values for the cursor. With entry of the value 100, the calculation of the dead zone gives nonzero velocity if the input from the joystick measurement is 0 to 100, or 155 to 255 in that direction. With the hardware I built for the external control box, a dead zone of 100 is a typical useful value; nonlinearities in the potentiometers make lower values impossible to use, and higher values make it very difficult to set the joystick to dead center and stop motion of the cursor. The variables ZD and DZ contain the dead zone limits.

The main routine of the color sketchpad program is found in the region from lines 1000 to 1070 of the listing. This "executive" loop begins with a small loop that scans for key input from the Apple II's keyboard. The current output of the keyboard is obtained by the magical incantation on line 1000. Two subroutines are called in this scanning loop at lines 1003 and 1005. The keyboard scanning loop waits until a valid key code (greater than 127) is returned from the keyboard before decoding a keyboard command. The subroutine at lines 3000 to 3350 blinks the cursor and reads the paddle, moving the cursor according to the values XX and YY which are input when the BLINK count has reached zero. The subroutines which implement motion are found at lines 6000, 6500, 7000, and 7500.

Returning to the main keyboard scanning loop, the second subroutine called within this loop is found at lines 8700 to 8820, and is responsible for reading the "DEPOSIT" switch, switch #2, and setting appropriate flags to perform the action of depositing a color. Eventually, at line 1010 a KEY value of an ASCII character code

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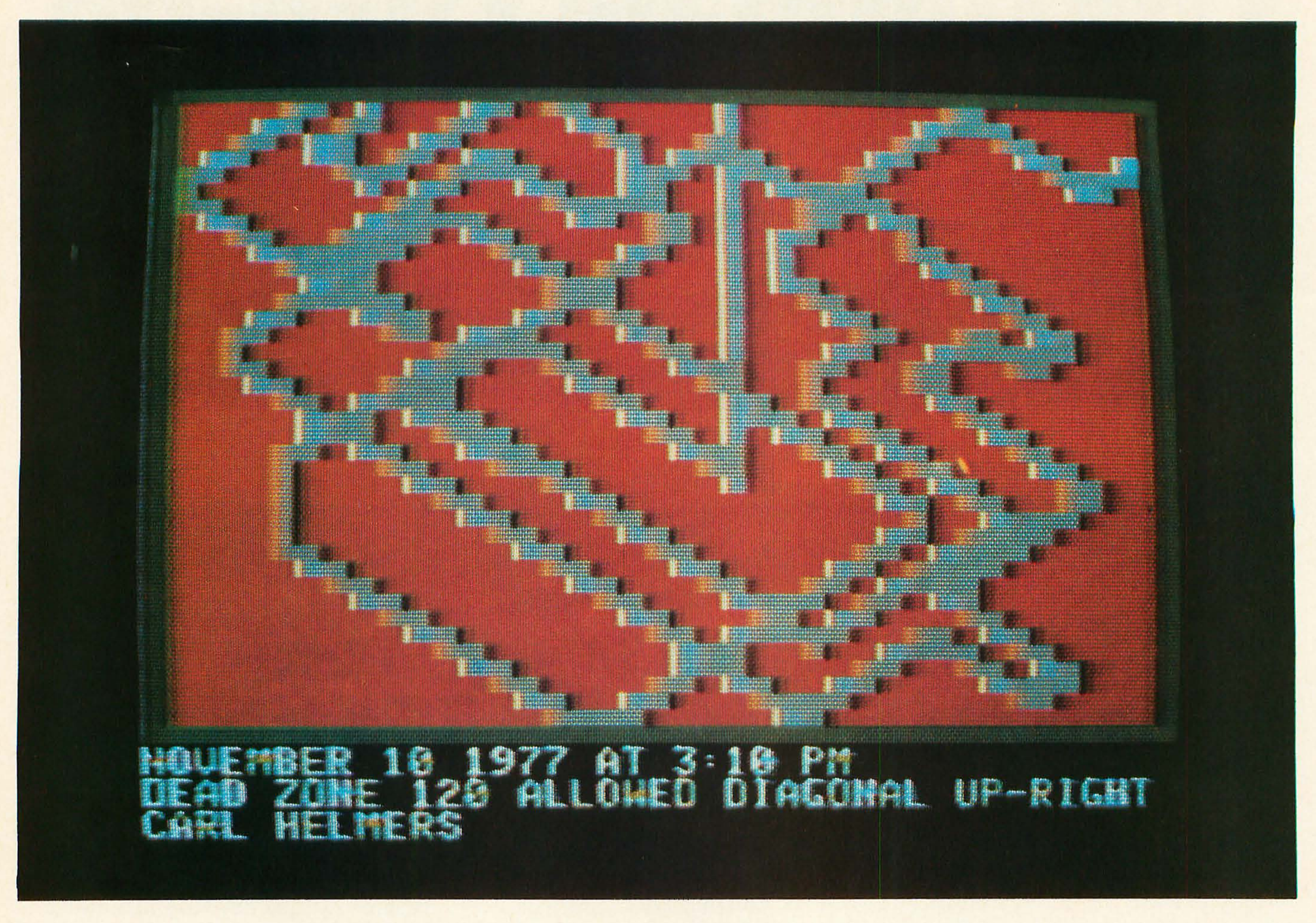


Photo 6: An example of another product of the color sketchpad program, in this case illustrating a text tag entered by the program's "T" command to identify when and who did the illustration. The comments on the second line of the text at the bottom refer to an experiment with the program's joystick dead zone parameter.

with a high order bit of "1" is detected in the range 128 to 255, and the inner keyboard scanning loop temporarily ends. Input of the KEY is acknowledged to the keyboard by the magical incantation to the hardware of POKE −16368,0 at line 1015. (All this hardware specific information was elicited from the documentation which came with the system.) After the KEY has been acknowledged, its value is checked and one of five command routines is chosen with a series of IF statements. If none of the valid commands is entered, the GOTO 1000 at line 1070 continues execution of the keyboard scanning loop looking for a valid command.

Turning to the implemented keyboard commands of this color sketchpad program, the "F" command is used to fill the screen with an arbitrary color. The details, found at lines 2000 to 2060, print a message to the user "FILL SCREEN WITH COLOR=" after which the user enters a value from 0 to 15 which is range limited by statements at 2020. (Thus if "F" is hit by mistake, typing an invalid color value outside the range 0 to 15 gets the user back to the main loop without erasing the current picture.) If a valid color is indicated, the screen is filled with that color, erasing all previous work.

The "C" command is used to access the routine starting at line 8500 which prompts the user for a new color value which will be used for drawing. The prompting message from an INPUT statement is "WHAT NEW COLOR?". As in most BASIC interpreters, the question mark comes from the INPUT statement's operation and the actual string found in the program has no question mark. The user response to this INPUT statement at line 8500 is a value limited to the range 0 to 15 by the assignment statement at line 8510 using the MOD function.

The "T" command is used to input a text tag contained in the string T$. This tag is typically output by a reference to the subroutine at line 2600 prior to resumption of the scanning loop after a command is executed. In the example of photo 6 the text tag was used to identify the date and time at which the picture was composed, and the "artist" responsible for it.

Finally, the "J" command is used to reset the joystick dead zone limits in the

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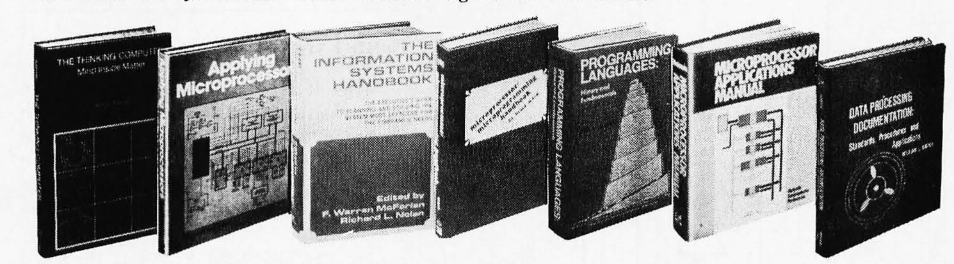
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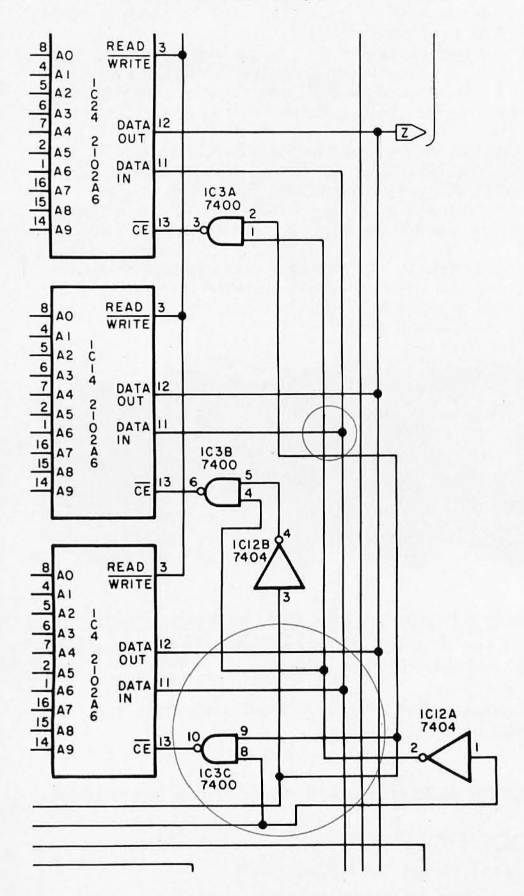
Summary of the Apple II

As noted at the beginning of this review, I was very enthusiastic about the prospect of this machine from the first word of its existence. To be sure, there are minor annoyances with this product in its present state, like the mechanical problems with respect to its case and keyboard mounting, and the persistent problems of radio frequency interference which I found using my particular color television set as the primary display. But such problems are minor compared to the achievements of this design.

Apple II is a well executed example of the way a personal "appliance" computer should be made circa 1977. It is suited for the relative beginner who knows BASIC but does not know hardware design, as well as for the advanced hacker who feels no qualms about using the system's documentation to create custom peripherals for the system. For the user who wants color graphics, the Apple II is the only practical choice available in the "appliance" computer class.■

BYTE's Bugs

A Flop in the Floppy



The drafting bug has bitten BYTE. The accompanying figure detail (taken from figure 1a of David Allen's article, "A Floppy Disk Interface," January 1978 BYTE, page 61, right-hand side) contains a number of drafting errors inadvertently included during the production of the article. The corrections are circled. In addition, IC18c, a three input AND gate, was incorrectly drawn as a NAND gate, and the A1 and A2 inputs of IC22 should be shown connected together. Our thanks to the readers who spotted these errors, and our apologies to David Allen.■

Clock Stops

I enjoyed M F Smith's article in the November 1977 BYTE on "Using Interrupts for Real Time Clocks." He did a great job in describing how to develop and use a real time clock. So I implemented his program on my AMI PROTO 6800 System, only to find it not functioning properly in updating the clock. After examing the program listing closer, I found the bug at line 29 of your listing on page 53. The index compare was only index by 7 into the constant table, it should be index by 8. After I made this change everything worked.■

William W Barncord
Burroughs Corporation
2473 S Memphis Way
Aurora CO 80013

Joystick Gets Stuck

This letter is in reference to "An Inexpensive Joystick Interface," which appeared in the March 1977 BYTE on page 88. I'd like to congratulate Tom Buschbach on a fine article, but there seem to be several mistakes in the schematic.

On the MC1408L-8, A1 is the most significant bit. The schematic shows this connected to the least significant bit of the counter. The eight digital inputs to the digital to analog converter should be reversed in order to obtain a proper sawtooth output.

Also, on IC2, 74193, the count up input is shown grounded. This must be held high to enable the count down input.

I have constructed this circuit using a different register chip (8212) and the above changes, and it works very nicely.■

William Lemiszki
424 Cambridge St
Allston MA 02134

Fractured Factors and Walsh Function Bugs

William Jackson's letter on page 172 of the October 1977 BYTE contains two errors which can be corrected by replacing the fourth equation with:

=(y+z) + j(x−z)

and the fifth equation with:

Where x=(a+b)c.

Regarding the September 1977 article "Walsh Functions: A Digital Fourier Series": in the third paragraph on page 196, one reads "Sin (11.25°) = 0.09802." The proper value is 0.19509. The value given is that appropriate for 11.25/2°. The sums should be, I think, 5.13842, −2.13578, −0.40974 and −1.03218 in table 4. The coefficients would then be 1, −0.4156, −0.0797 and −0.2009. Also the signs for SAL(7) at the bottom of the table should be PNPNNPNP. What was printed is CAL(7).

If I have not made a mistake, the resistors in table 5 would be unchanged, but shouldn't there be some differences in the circuit diagram?

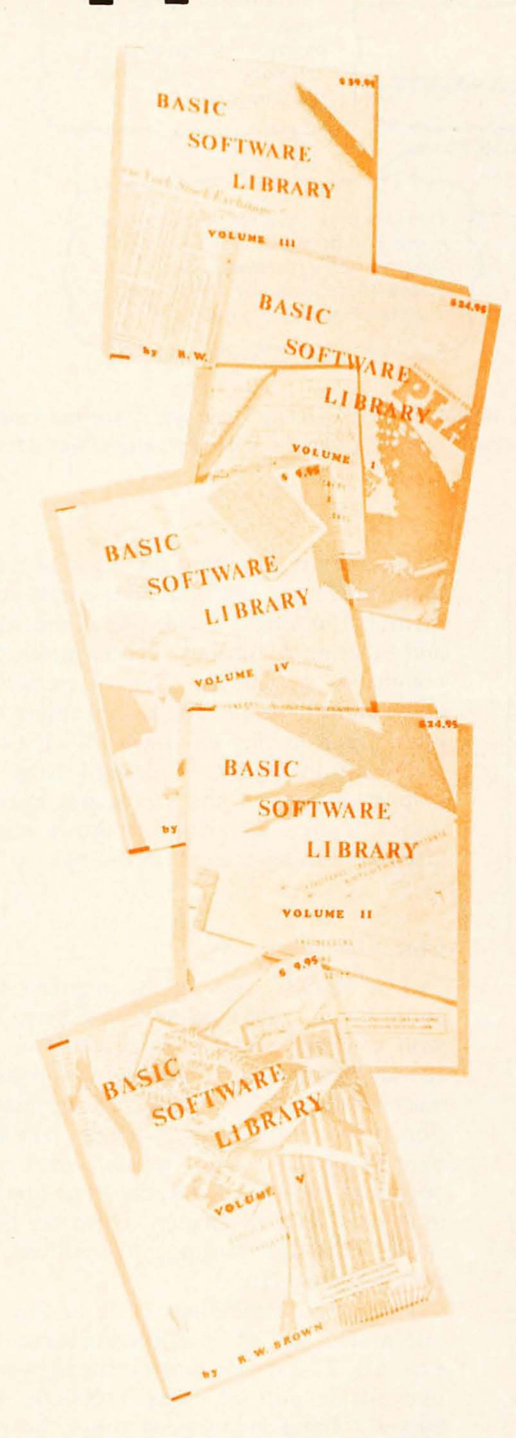
J S Lefson
6609 Cote St Luc Rd, Apt 203
Montreal, Quebec
CANADA H4V 1G9

Dr Jacoby replies:

Mr Lefson is correct that SAL(7) in table 4 is misprinted. This can be easily seen by comparison to table 3 or by knowing that the SAL functions themselves are odd about their centers and even about their 1/4 and 3/4 period points, and thus should give identical values to the left and right of center in table 4.

In addition, the values for Sin 78.75° and Sin 101.25° are incorrect and should read 0.98078. I believe that the values for the sums are correct as given as well as the circuit connections [compare to figure 3 for SAL(7)]. One point of confusion here might be the signs of the coefficients, since they take into account the inverting *op amp configuration and thus appear reversed.*■

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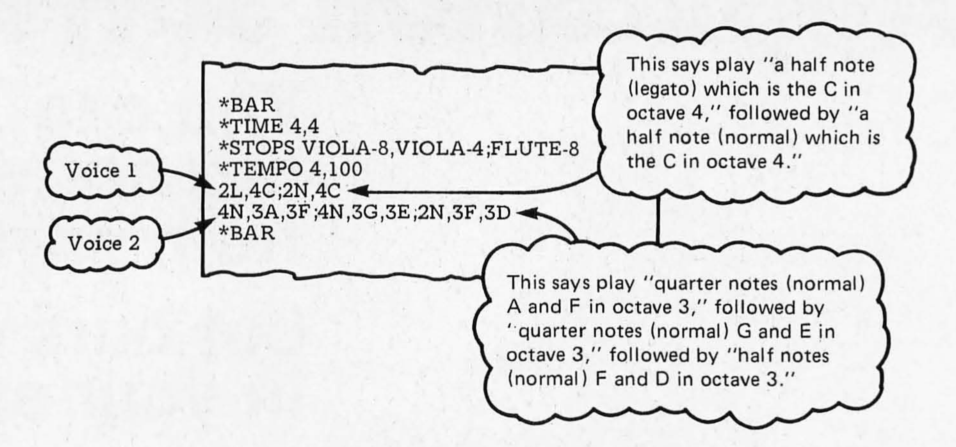
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Continued from page 12



Listing 1: The musical example of figure 5 written in the MUSIC language. "Normal" means that there is to be a slight pause between notes. "Legato" indicates a smooth transition with no gaps.

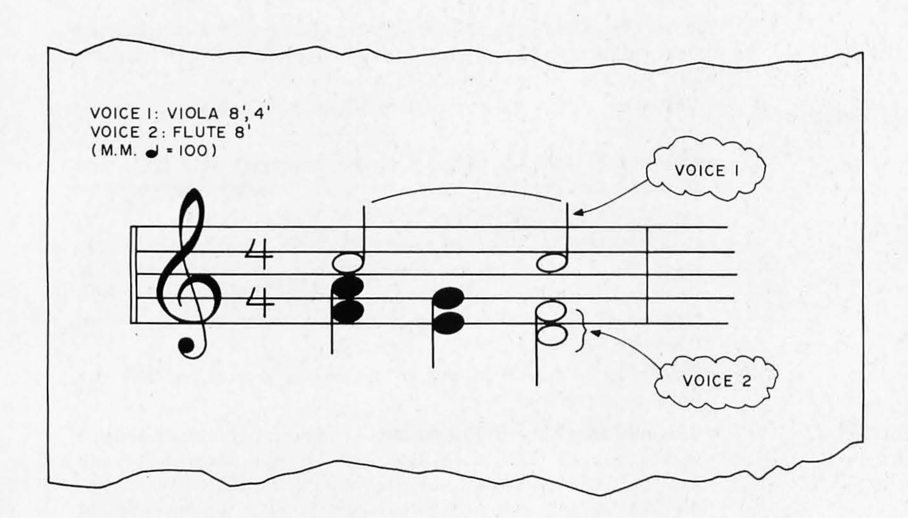


Figure 5: An example of how musical notation is represented in the MUSIC language.

The Music Editor

An editor is a program that allows a user to easily create and modify files (which of course may be programs). The Music Editor is a program that allows composers to graphically create and modify MUSIC language programs. The Music Editor is written in Altair Extended BASIC 4.0 and runs on the Altair 8800b system using a Magnavox plasma display terminal.

At the simplest level, the editor allows the user to type in and alter statements like any text editor. It also permits the user to copy or move blocks of statements. The editor verifies the syntax of each statement entered.

At a higher level, the editor can be used to graphically display and edit data statements. When entering this level, the editor draws the staves. If an existing data statement is to be altered, the notes of this data statement are drawn; otherwise the staves will be empty, awaiting the input of a new data statement. The user edits a data statement by moving a cursor about the staves and entering commands. Special macro-like commands permit the user to create and copy chords, delete events and insert new ones. Upon leaving this higher level, a data statement in MUSIC is derived from the graphic display of the staves and inserted into a scratch file. Photo 3 shows what a graphics editing session looks like to the user.

Object Language

The MUSIC language is compiled into code for a "make-believe" machine, one with a simple set of instructions. Thus we can say that the object language is in pseudo-machine code. Each object language instruction is two 8 bit bytes in length. The first byte in each instruction is interpreted as an operation code (op code); the second byte is used as a data parameter. There are three classes of object language instructions: set port, wait, and repeat.

Op codes with values of 0 to 253 are interpreted as set port instructions. For example, 27-3 means turn on the right-most two bits in port 27 (since 3=00000011 in binary). These instructions cause the data byte to be deposited in the port number given by the op code itself (each latching port has a unique address). The bit pattern of the data byte specifies which pipe valves attached to that port are to be opened and which ones are to be closed. The pipe valves will remain in that state until they are reset by another set port instruction.

Repeat instructions (op code value of 254) are trapped by the master system. The master processor handles repeats by retransmitting parts of the object program to the slave



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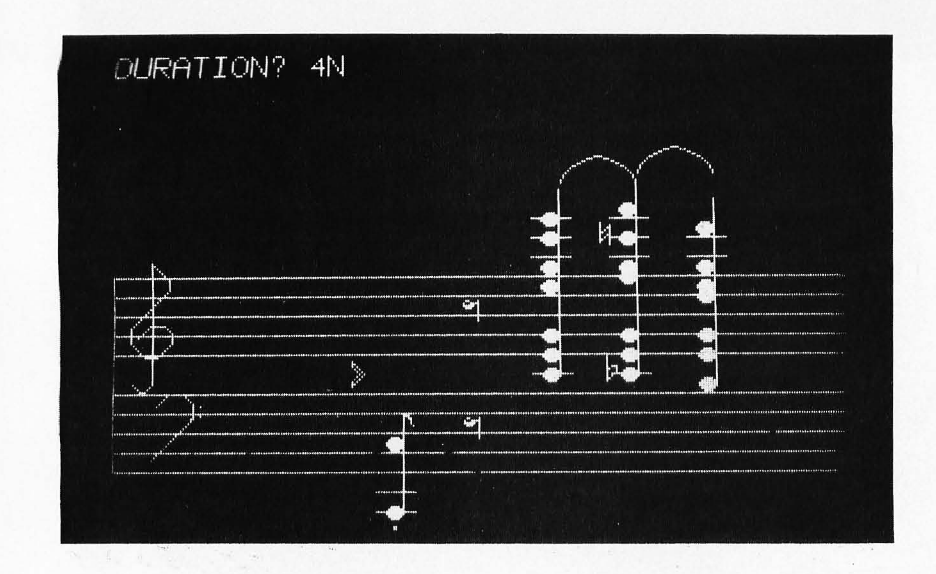


Photo 3: The authors' Magnavox plasma display terminal during an editing session. Notes and chords can be created or modified by moving a cursor to the desired position. Entire musical phrases can be copied if desired. Chords or whole measures that repeat need be entered only once.

Voice 1

48	The note 4C is 48 half tones up from C_0
–3000	A legato half note gets a timing of 3000 units
48	This is the second C
–2400	Timing for a normal half note
–600	Pause after a normal half note

Voice 2

45	This is 3A
41	This is 3F
–1200	Timing for a normal quarter note
–300	Pause
43	This is 3G
40	This is 3E
–1200	Timing for a normal quarter note
–300	Pause
41	This is 3F
38	This is 3D
–2400	Timing for a normal half note
–600	Pause

Listing 2a: An example of how the program in listing 1 is compiled in MUSIC. The first step is error checking, followed by the production of intermediate code for each voice.

This means turn on the bit pattern for 4 in Port 12:

PORT 12 | 00000100 |

This bit goes to 4C in the viola rank.

12	4	C from Voice 1 on 8 ft viola
14	1	C from Voice 1 on 4 ft viola
27	32	The F-A chord in Voice 2 on 8 ft flute
28	2	
255	48	Wait for 480 ms
27	0	Clear the chord in Voice 2
28	0	
255	12	Pause 120 ms (space between chords)
27	144	The E-G chord in Voice 2 on 8 ft flute
255	48	.
27	0	.
255	12	.
27	36	etc.
255	96	.
12	0	.
14	0	.
27	0	
255	24	

This says turn on the bit pattern for 144=128+16 in Port 27:

PORT 27 | 10010000 |

This bit goes to 3G in the flute rank. This bit goes to 3E in the flute rank.

Listing 2b: Here the compiler combines the voices in listing 2a to produce the final object code.

processor as specified by the data byte of the repeat instruction.

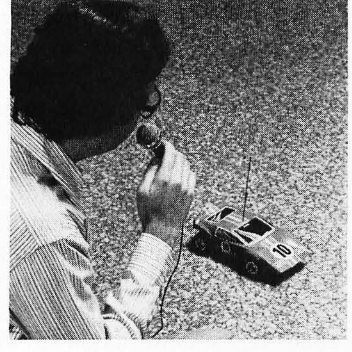
The wait instruction has an op code value of 255. The second byte of the instruction is interpreted as a nonnegative integer. This byte's value fixes a delay period computed in 10 ms units. For example, 255-60 means wait 600 ms.

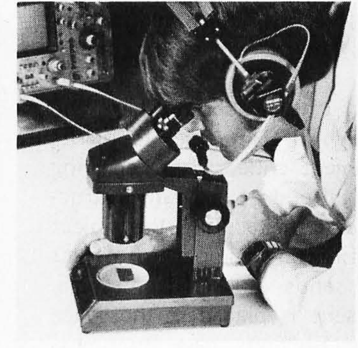
An object program consists of a series of "frames." Each frame contains zero or more set port instructions and is terminated by a wait instruction. A frame is executed by the slave computer by first executing all set port instructions in a frame almost simultaneously. The set port instructions cause some pipes to be turned on and others to be turned off. If a particular port is not addressed by any set port instruction during a frame, this port's pipes remain in their current state. This new pipe state lasts for the duration given by the frame's wait instruction. At the end of this duration, the next frame's execution begins. Thus each frame causes a combination of pipes to be played for a set length of time. An example of an object program is given in listings 2a and 2b.

The execution of the object program is controlled by two performance programs that couple the master and the slave computers together. There are two reasons why we decided to use a pair of computers to handle the performance of the music: one, the correct latching output ports were already available on the Intellec, and, two, the slave could handle all the real time demands while the master handled the retrieval and loading of "pages" of the score from the diskette. (A page is defined as 256 bytes of object code.)

The slave microcomputer's memory acts as a circular buffer. The master initiates an object program execution by sending a

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header message to the slave. The master then waits for a Block Request (BR) message. At the receipt of each BR message, another page (256 bytes) of the object program is sent to the slave.

After receiving the header message, the slave sends enough BR messages to fill its memory with object code. After receiving enough pages or an end of program instruction, the slave starts executing the object program. After finishing one page of object code, the slave sends out a BR message. The next page sent is placed in the space released by the previous page that was executed. The execution of the object program and the refilling of the buffer proceed concurrently.

After sending the entire object program, the master processor ignores all further Block Request messages. When the slave executes the end of program instruction (which is a WAIT instruction with duration zero), it sends a completion message back to the master processor. The master processor can then inform the user that the slave is ready to accept another program.

This performance system software consists of two programs. The "slave" program is written in Intel 8080 assembly language. Its machine code representation is stored on read only memory in the slave microcomputer. The "master" performance program is written in Extended BASIC 4.0 for the Altair 8800b computer.

The Compiler

The compiler accepts a MUSIC language program and outputs an annotated listing file. If no errors are detected, an object program is then generated and saved on a diskette as a file. Thus the compiler's work can be divided into two phases: error checking and code generation.

The error checking consists of two types of operations: syntax verifying and context checking. A syntax verifier examines each statement to insure that it conforms to the rules of the language. For context commands it checks for correct number and types of arguments and correct placement of this statement in the measure. The repeat command's arguments and placement are checked and the nesting of these statements is verified. Data statement arguments are checked for syntax correctness.

In addition to syntax, the context correctness of data statements is checked. The number of data statements in a measure must equal the number of voices currently active as declared by the last STOPS command encountered in the program. The duration of each data statement must equal the measure duration as declared in the currently active time signature. This checking is a real help to the composer since it handles all the petty details.

The code generation phase of the compiler is divided into four operations: generating repeat instructions, handling context commands, processing data statements, and coordinating measures.

Each repeat command causes one object code repeat instruction to be generated. Repeat instructions cause all the data between HEAD and TAIL commands to be used twice.

The context commands serve a function similar to declaration statements in conventional computer languages. Their main function is to alter the values of the global arrays and variables that determine the note address and note timing calculations. A note address is a number that relates a note to a pipe, while a timing determines how many milliseconds the associated notes are to be held.

The data statement handler processes the data statements to determine the notes to be played for a particular measure. Each voice has its own First-In-First-Out (FIFO) queue for storing information about the events of the current measure. As each event in a voice's data statement is processed, its FIFO queue is filled from the top down. First the notes of the event, then the duration of the event, and finally the duration of the pause between this event and the next one are placed on the queue. At this stage, note values are stored as integer numbers representing a number of semitones above a base pitch, without regard to stop settings. The durations are computed in basic time units regardless of the current tempo setting. The durations are stored as negative numbers in order to distinguish them from note values. Figure 6 shows the general format of a queue for one voice. It represents a sequence of four chords with a rest between the last two.

In this example there is no pause duration between events 2 and 3, indicating that event 2 is played legato with event 3. Event 4 has no note values, therefore it is a rest. Glissandos and tremolos are treated like event macros. They are translated into a series of events by the data statement parser before they are processed onto the queue.

After each voice in a measure has been

parsed, the voice coordination routine generates the object code using the following algorithm:

1. The duration counter for each active voice is set to 0.
2. The duration counter for each voice is examined. Those voices with a zeroed duration counter have their top sequence removed from their queue for processing. (A sequence is all the information from the top of the queue down to and including the first duration of pause found.) The sequence's duration is stored in the voice's duration counter.
3. The voice's bit map is cleared. (The bit map is an array of bits where one bit is used to represent the state of one organ pipe.) As each note value of a voice's sequence is processed, it is expanded into as many note addresses as the number of stop settings defined for that voice. Each note address generated causes a particular bit in the voice's bit map to be set to 1.
4. All the voice bit maps are ORed into a master bit map.
5. The master bit map is compared to the previous master bit map.
6. Those output ports whose bit pattern has changed generate set port instructions with the port's new bit pattern as the data byte of that instruction.
7. To generate the wait instruction, the duration counter for each voice is examined and the minimum duration is found. This minimum duration is subtracted from each voice's duration counter.
8. The minimum duration is multiplied by the tempo variable to yield the actual timing of the object code frame produced. If a frame is within an accelerando or ritard passage, the timing is altered to reflect the gradual change in tempo, the tempo variable is updated, and the duration remaining in the tempo changing passage is decremented. The final actual timing is used to produce a WAIT object code instruction.
9. The current master bit map is labeled as the previous master bit map.
10. The routine now goes back to step 2 if all the queues are not empty; otherwise the next measure in the MUSIC language program is processed.

The queues should empty simultaneously since each voice's data statement should have a duration equal to the one set by the time signature. (This is checked during phase 1 of the compiler.)

The above algorithm was designed to compile multivoice music efficiently. An important feature of this algorithm is that it allows more than one voice to share the same rank of pipes. In addition, it permits the user to generate from each note specified many pitches through the stop setting mechanism. Since the stop settings are performed through software, a user can transpose each note of a voice any number of tones and into any rank of pipes. Listings 2a and 2b show how the above algorithm works for the simple two voice example given in figure 5.

Future Plans

While the system described here is not meant to compete with large dedicated music research systems, it nevertheless has several advantages over a number of other computer controlled music systems. Currently, we have two ranks of pipes with 64 pipes in each rank. However, additional ranks of pipes could easily be added to the system. Each 64 pipe rank requires only eight more latching output ports. The theoretical limit for an Intel 8080 based system is over 2000 pipes. Microcomputers that use memory mapped IO could conceivably control hundreds of thousands of pipes.

The system can be extended to other musical instruments. By using solenoids, any keyboard instrument can be controlled through the output ports. Alternatively, the solenoids might be placed inside the instrument, driving something like the jacks in a harpsichord directly. To play the harpsichord along with the organ would just require the addition of a harpsichord stop to the MUSIC language.

Electronic synthesizer music is not incorporated in our system because of the high cost of the special hardware needed, but at least three low cost analog output boards designed for Altair (S-100) bus microcomputers have recently been announced. It seems reasonable to expect that the MUSIC language could be applied to these new pieces of hardware.

The voice concept has some application to "synthetic" music composition because it allows the user to create new timbres by specifying nonstandard overtone ranks (eg:

```
chord   { note
          note
          note            event 1
          duration
          pause }

chord   { note
          note
          note            event 2
          duration }

chord   { note
          note            event 3
          duration
          pause }

rest    { duration }      event 4

chord   { note
          note
          note            event 5
          duration
          pause }
```

Figure 6: The general format of a queue for one voice used in the MUSIC language.



a 3.1416 foot flute). By assigning dummy stop settings to certain voices, the composer can also isolate the effect of these harmonics during a test performance.

We are planning to eliminate the need to compile and save object programs. An assembly language version of the compiler is being written that will interpret MUSIC language programs in real time. This will be done by sending the bit pattern computed in step 6 of the measure coordinating routine to the designated output port and use the time value generated in step 8 to set an interval timer. This new software system will allow a user to interact with a performance. We also hope to build a subsystem to capture keyboard performance and translate it into a MUSIC language program.

Aside from musical application, the programs written for this system can be used as a realistic basis for explaining many important concepts of computer science in a context that removes much of the mystery surrounding computing. In many ways, this could be the most useful contribution of the music system, suggesting as it does that the teaching of complex ideas has much to gain from a liaison with the creative arts.■

A Glossary of Some Musical Terms

Accelerando: A direction telling the musician to make the music gradually faster (increase tempo).

Bar: Vertical line on the musical staff separating the measures of music. Sometimes used as a synonym for a measure.

Glissando: A rapid sliding up or down the musical scale.

Key Signature: The sharps or flats placed after a musical clef to indicate the key.

Legato: A direction telling the musician to play in a smooth and connected manner.

Ritard: A direction telling the musician to make the music gradually slower (decrease tempo).

Semitone: The interval between two tones in the chromatic (well tempered) scale (ie: the distance between A♭ and A is a semitone).

Staccato: In a broken or clipped manner.

Tremolo: Effect produced by the rapid repetition of a note.

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The Microcomputer and the Pipe Organ

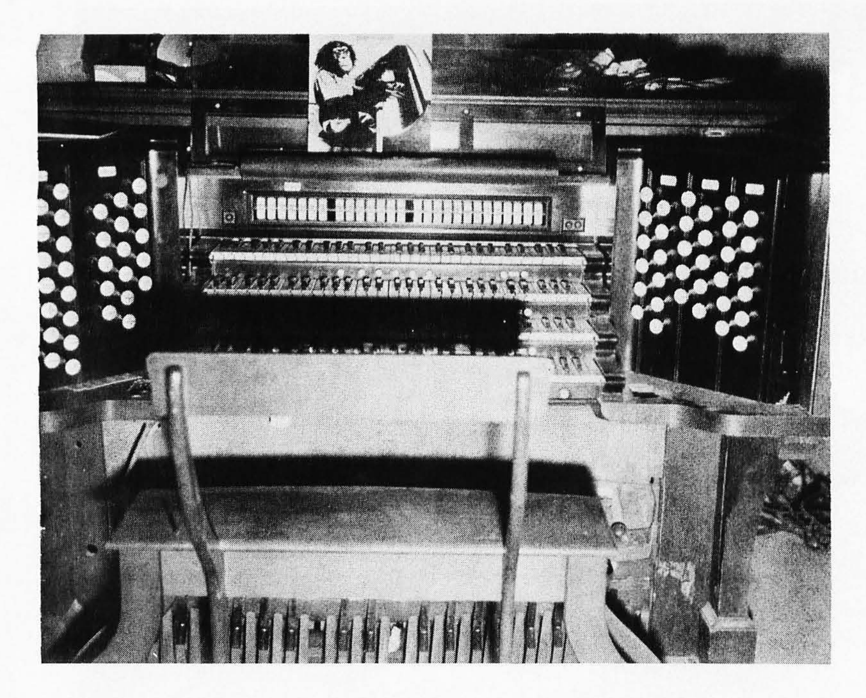


Photo 1: Pipe organ console shown in the home of the author's colleague, Jim Brennan, who did the custom installation work. The console was obtained from a church in Pasadena CA.

One night I got a call from a man who had been wandering through the personal computer stores in the area. He was looking for a computer to operate his huge pipe organ. Inevitably, he was given my phone number, since I had been going around to the same stores telling everyone that I was working on a controller for my pipe organ.

There are several gimmicky reasons for wanting to attach a computer to an organ. My reason is that the combination can provide the performer with a more flexible, easier to play instrument. And then there are all those gimmicks. As it turns out, using a microcomputer can be less expensive than conventional console wiring. Before we get into the subject too deeply, the "organization" of the king of instruments should be made clear.

The performer sits at the *console*. The performer's hands rest on one or more keyboards called *manuals*. There are usually from two to four manuals. The feet play on a set of keys placed beneath the bench called the *pedals*. On most organs since the late 1800s, the console is separate from the rest of the instrument and is connected to it by means of electrical cables. As with the computer, the console is the "command center" of the instrument. In addition to the keyboards there are a number of other controls on the console that will be discussed later.

Blockflotes and Zimbels

The sounding portion of the organ consists of many pipes. Each pipe sounds one note. There are typically many different pipes for a given note, each of which has a different sound quality or *timbre*. A set of pipes, all of similar timbre, one for each key on a manual, is called a *rank*. Each rank has a name, many of which are hallowed by centuries of use. Some, like *diapason* (dia *pay* zen) or *bourdon* describe sounds that are characteristic of organs and nothing else. Others, such as *trompette* or *blockflote* are reminiscent of trumpets and wooden flutes, respectively. Obviously one rank is a minimum for an organ. (Renaissance *portative* organs had one rank.) A small organ usually has three or four ranks, controlled from two manuals. The one being installed in my house has 26 ranks. A large organ will have 70 or more. The organ owned by my friend mentioned above has 140 ranks. That is very large, and only a few cathedrals have more.

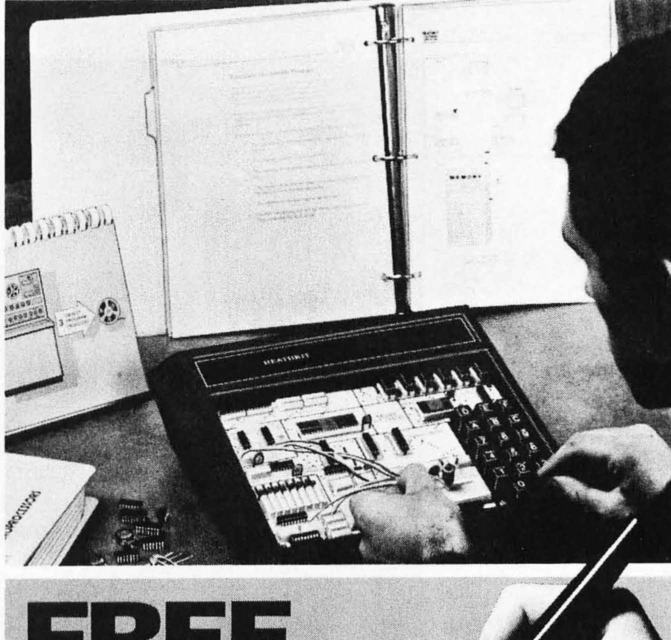
Each rank has 61 pipes, as there are 61 notes on a manual. Thus for a pipe organ of a 100 ranks there are 6,100 pipes. Each rank is turned off or on by a knob or switch labelled with the rank's name. These knobs are called *stops*. (The terms stop and rank are sometimes used interchangeably, but in this discussion rank will refer to a set of pipes, and stop to the controlling knob.)

A large organ often has four manuals (named great, swell, choir and echo or positiv) each having 61 keys, a 32 note pedalboard, 100 or so stop knobs, and a few dozen assorted controls. Thus there are about 500 controls that the organist must manipulate: a complicated instrument, indeed.

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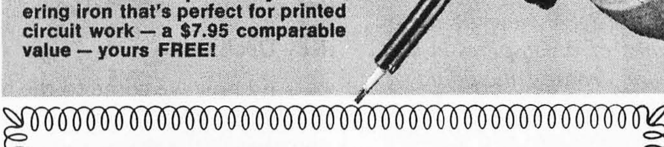
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Photo 2: A view of three ranks of organ pipes in the living room, including a Rauschepfeife, left, Holtzregal, center, and Zimbel bass on the right. Each rank has its own particular tonal color.

Key Decisions

And now we come to the microcomputer. It must keep constant watch on 500 switches and control some 6,000 relays, one for each pipe. It must never miss a switch closure or release, and must operate the correct pipes (sometimes dozens simultaneously) within 1/20 of a second. Is this within the capabilities of an 8080? As it happens, it is. But not without a bit of tricky IO design and some swift algorithms.

For completeness, it should be mentioned that some ranks are not exactly 61 notes. "Unified" ranks often have 75 pipes, and some special ranks have fewer than 61. But fortunately these exceptions are easily handled. The problem is simplified in some organs (a little) by sets of ranks grouped into "straight" *chests*. Instead of each pipe having its own electrically operated valve (a "unit" chest), each rank in the chest has a valve. Then all notes of the same name (such as all Cs or all F#s) have one valve. This loses some generality, but requires fewer valves and electrical connections. For M ranks of N notes each, a "straight" chest requires M+N valves. A "unit" chest has MxN valves.

Organs also traditionally have *couplers*, which operate either within a keyboard or between keyboards. An intermanual coupler has the effect of operating a note on one manual when you press the corresponding note on another. (On some old organs both keys actually move when you press one of them. This may have given rise to "phantom of the opera" stories.) A coupler that works within a keyboard plays a note typically one octave higher or lower than the key you are playing, but on the same keyboard. Intervals other than an octave are also available on some organs.

An organ is also separated into *divisions*. These have the same names as the manuals: typically, great, swell, choir, echo and positiv. The pipes played by the pedals form another division: the pedal division. Each rank belongs to exactly one division. In the traditional organ, a manual can play pipes only in its division. You can couple manuals together, but it is impossible to play a rank in the swell division from the great manual without playing *all* stops that are pulled in the swell division from the great manual. This separation into divisions has no musical benefits, but is done merely to simplify the construction of the switching in the console. By means of a microcomputer, divisions can be eliminated. The organist can then independently assign any rank to any keyboard. This is the first of a number of nongimmick improvements that can be appreciated by any organist.

The switching in the traditional organ is done by the most incredible collection of electrical, mechanical and pneumatic switches imaginable. That it works at all, being made mostly of slats of wood and strips of leather with silver wires for contacts, seems miraculous. It is not surprising, then, that freedom in interconnection has been restricted in the past.

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reminds one of a cross between the innards of a computer before the mother board was invented and a telephone company switching office. A major advantage of the computerized organ is the elimination of most of this wiring. In a very large organ, the cost of the computer system may be *less* than the cost of the cabling alone.

When an organist plays a piece, it has a characteristic sound quality produced by a judiciously selected set of stops being activated. A particular collection of stops is called a *registration*. It is usually desirable to be able to store such combinations. There are a number of buttons called *pistons* which recall combinations of stops. Logically enough these collections of stops are called *combinations* or *presets*. There are often a few fixed presets, and a number of pistons are provided whose registration the organist can change at will. Another advantage of the computer controlled organ is that many more presets are available. 4 K bytes of memory can store hundreds of different presets, more than on any conventional organ. This amount of memory costs less than one preset done mechanically! And it's a lot easier to install.

Consider what happens when a single key is pressed. First, any keys that are coupled to it are also activated on its keyboard as well as on other keyboards. For each of those resultant keys, as well as the original key, the applicable stops must be looked up. If there are two couplers and four stops activated for each of the three keyboards involved, no less than 12 pipes must sound. When playing a full chord with many couplers and stops engaged, it is not uncommon for 500 pipes to be operated simultaneously.

Getting Organized

A number of schemes were concocted for driving the pipes and reading the keys. One scheme, which has been used on smaller organs for computer control, was to have each key send out a unique code. Each pipe recognizes its own address. The computer would receive key codes as well as stop and coupler codes, and compute the appropriate pipe addresses. A decoder at each pipe, as well as a diode matrix or other encoder for the console, would be required. Since on a large organ there are over 2^{12} pipes, even a 12 bit code would not be long enough. This would mean assembling two 8 bit words for each pipe. Putting out over 500 of these in 1/30 of a second (considering the number of steps required in the program) would have been impossible. Further, the cost for decoders at each pipe is prohibitive. This ruled out going to a 16 bit computer, since it wouldn't help the decoder problem, and a larger word size seemed to hold few advantages in any other way.

Cost alone ruled out the brute force approach of using a very fast computer. Another way to get high data rates from a microcomputer would be to use direct memory access (DMA) circuitry. With this scheme one DMA device scans the keyboard continuously and enters key depression and release information into memory. The main processor (at its own rate) scans the keyboard image in memory and constructs a list of pipes to be played or quieted. Another DMA scans the list of pipes and controls the pipes accordingly. In essence, three computers would share the same memory and would run asynchronously, each going as fast as conditions allowed. This seemed feasible, and is necessary for larger organs. But for smaller organs the DMA is not needed, as will be seen.

Part of the solution lay in hardware. At one extreme of decoding (as explained above), each pipe has its own decoder. It would be more efficient for each group of, say, eight pipes to have a decoder which detects its code and then accepts the next byte as controlling eight pipes in *parallel*. The 8 bit control byte 10001001 would mean that the notes C, E and G are to be played, while leaving C#, D, D#, F and F# silent. This would reduce the number of decoders by a factor of 8, and then operates eight pipes at a time. This was fast enough in the IO department, but the time required to assemble the control bytes by masking or rotation was too great. A microcomputer handles bytes with great efficiency, but manipulating individual bits takes significantly more time. A number of algorithms were considered, but it was apparent that they were not suitable.

At the other extreme from a decoder for each pipe is the idea of having no decoders whatever. This idea was put forward early in the design effort, but was discarded as ridiculous. In the end it became clear that the idea was not only feasible, but fast and cheap to implement in hardware. It also made the software much easier to design. It works like this: A very long serial-in/parallel-out shift register is made. It will have at least one output for each pipe. Using available 8 bit shift registers, the 140 rank organ's 2000 electrically operated valves require about 250 shift registers. (The 7000 pipes require only 2000 controlling lines since most of them are on straight chests.) In effect we build a 2000+ bit shift register, a long "tube" through which 1s and

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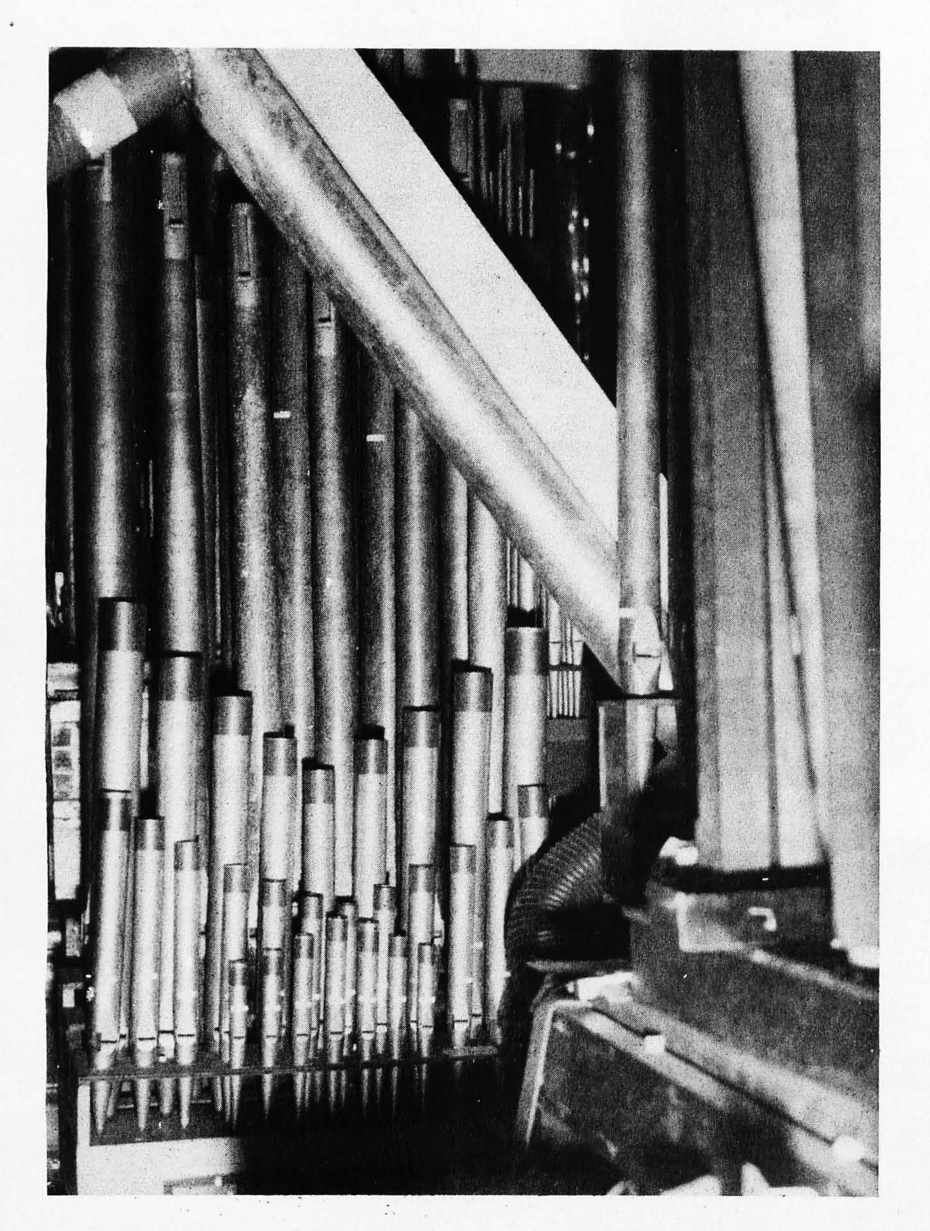
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0s flow in single file. When all the 1s and 0s (standing for pipes sounding or silent) reach their correct positions, a command (strobe) is sent operating *all the pipes at once*. If the process is to take 1/60 of a second, the shift register has to move 2000 bits in that time. But this is a rate of 120,000 bits per second (120 kHz) which is within the capabilities of the shift register and the computer but a bit beyond an unaided 8080. Remember that these calculations are for a mammoth size organ. Most organs are significantly smaller and the problems are correspondingly easier.

A similar approach is used for the keyboards. There exists a 33 input parallel to serial converter made for electronic organs. Just two of these integrated circuits would suffice to encode an entire manual. The 500 controls could be transmitted serially to the computer in 1/200 of a second at 100 kHz. The interface would require fewer than 20 "critters." Again, this is for a huge organ. My own home organ would require only ten integrated circuit chips for its console.

Photo 3: Another view of the organ showing the swell chest and echo chest.



The hardware for a large organ can now be summarized. A 500 bit parallel to serial converter for input, a 2000 bit serial to parallel converter for output, one input port and one output port are required. Each pipe also needs a power transistor to handle the 0.5 A at 14 V required by the valves (this is a typical figure). Some of the larger pipes might require two stages or a Darlington power transistor, but there is no real difficulty in the design. Another side benefit accrues at this point: Many pipe organs use electro-pneumatic valves for each large pipe. This is because an all electric valve opens too suddenly. To solve the problem, the traditional builders designed the electrical valve to let air into a small bellows which, in turn, operates the valve that lets air into the pipe. A pair of resistor-capacitor (RC) networks and a diode in the base circuit of the power amplifier for each pipe can give the desired slow attack and release usually obtained by the much more expensive and problematical pneumatic system. This can amount to savings of over $1000 in a large organ. It should be mentioned that some organ manufacturers have been successful in making satisfactory all electric valves with appropriate attack and decay curves. They would not require the RC networks.

Software design was as gradual as the hardware design. There were two breakthroughs necessary before it was clear that the 8080 could work quickly enough. (When this design was being done, by the way, the Z-80 and other faster processors were not yet in production.) But the constraints of the 8080 and the very large organ forced a much tighter and more clever design than would have been developed if we had had more powerful computers and a smaller organ. Given the newer computers, of course, larger and more complex pieces of equipment can be controlled. Many industrial plants have fewer than 200 sensors and 2000 elements that need to be operated in real time. A microcomputer using the techniques outlined here could handle them.

The program begins by sweeping in the console settings. To save time only *one bit per word* is used. This wastes 7/8ths of 500 words, but memory is cheap. The same trick can be used in output, eliminating the necessity to pack bits into bytes. Thus over one byte per key and one byte per pipe will be sacrificed to gain speed. That amounts to $40 at most in memory costs. It buys us

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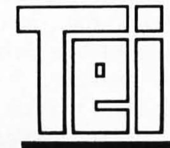
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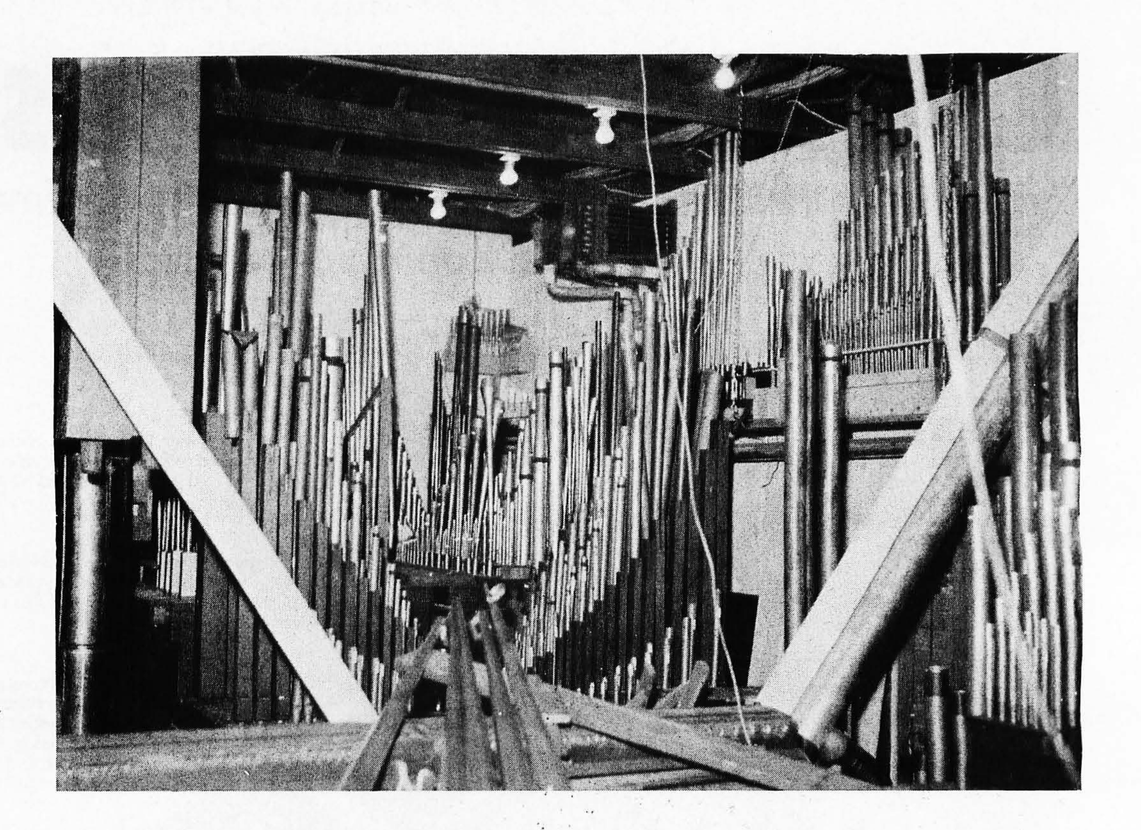


Photo 4: The main organ chamber with portions of an organ taken from a Sacramento church.

speed and simplicity, and it is worth it. While it now seems obvious that this is a useful way to proceed, it somehow took four months to find the solution. This is probably because we are so reluctant to waste memory. A pipe organ costs from $20,000 to whatever you care to spend (a million dollars is not unusual). The computer costs are lost in the small change.

For a small organ, the DMA is not even needed, and the input and output loops are very simple:

1. Point to a memory location.
2. Do an input (or output).
3. Move the contents of the accumulator to that location.
4. Increment the location.
5. Check for done. If not done, do an input (or output), etc.

The loop can be done on an 8080A at 66 kHz. Thus, an entire 20 rank organ can be updated in less than 0.02 second. The DMA would do the same algorithm, but at 1 MHz, and would overlap processing. The 8080 with a 2 MHz clock is just fast enough. An 8085 or Z-80 processor would be more than fast enough. Again, remember that for a typical home or small church organ, the plain old 8080 would have the necessary speed and that we are discussing a worst case design.

Even with IO solved, there still remains the problem of deciding which pipes are to go on and which to go off. At first this was a stumbling block in terms of the time it would take to do the computations. On each console scan, it seemed, a table of couplers would have to be made up, as well as a table of stops. A key depression, through the couplers, results in a number of "virtual" key depressions. Since some virtual keys, being higher or lower on the keyboard than the original key, will go off the end of a keyboard, they must be deleted from the virtual key list. The remaining keys then have to be processed through the stop list to determine which pipes are to be played. Since the IO routines take a total of about 0.04 seconds already, the processing itself must take no more than 0.013 seconds. Just the checking for out of range virtual keys would take more time than we can spare.

The easiest solution to the coupler spillover problem is to include a few extra places in the shift register on both ends of each rank. This allows all the ranks to have the same shift register length whatever the actual number of pipes. The first advantage is that out of range virtual key depressions need not be checked for, since they fall into unused sections of the shift register. As with the wasted memory, the cost of the unused shift registers is small. The second advantage is that the electronics for every rank, of whatever kind, can be mass-produced. This makes it less expensive to build, as well as making the software easier to write (aside from merely being faster).

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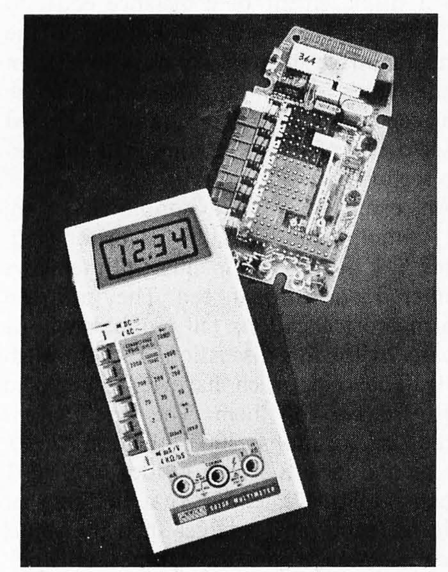
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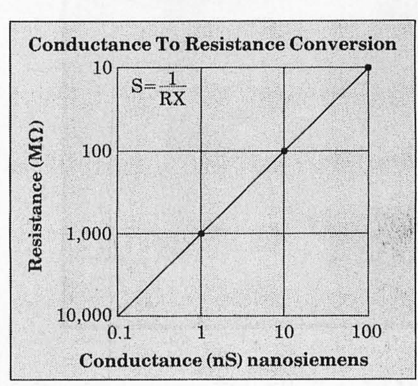
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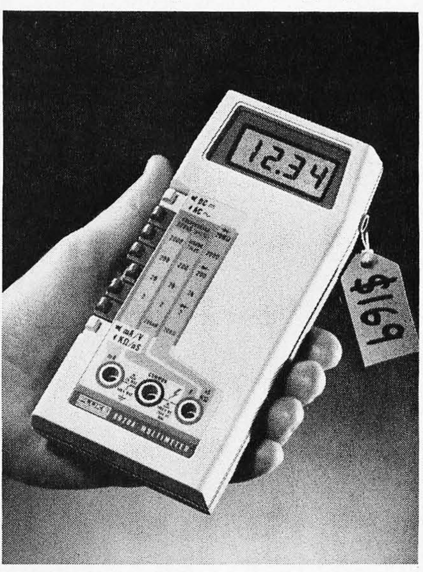
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1808-7101

Circle 47 on inquiry card.

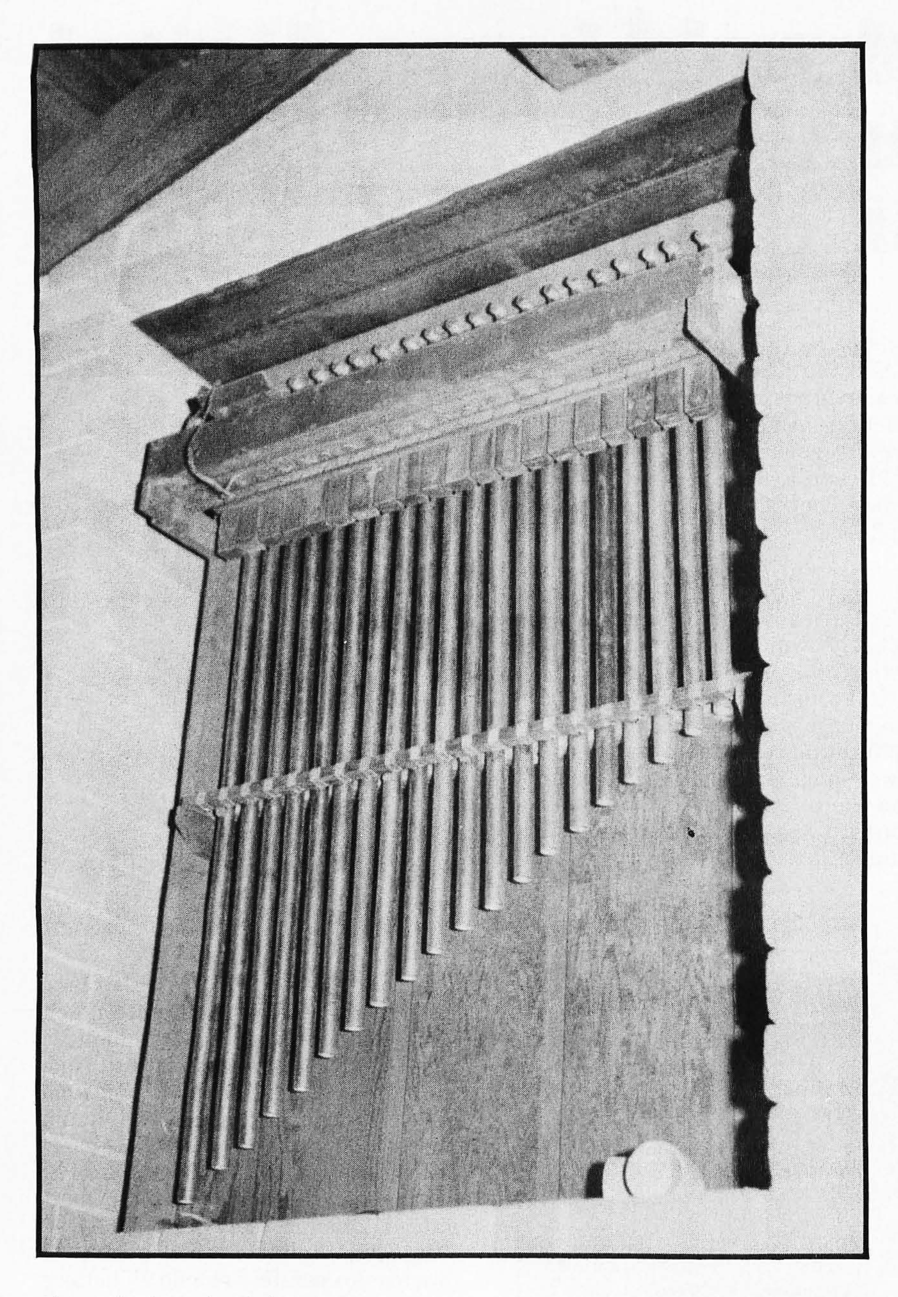


Photo 5: A rank of chimes pipes.

Except to satisfy traditional organists, there is no reason to have intermanual couplers on a computer controlled pipe organ. The original reason for including intermanual couplers was to minimize the limitations imposed by the separation of the pipes into divisions. The computer, by being able to assign any rank to any manual (or to the pedals), eliminates the need for these couplers. They might well be eliminated in my own organ.

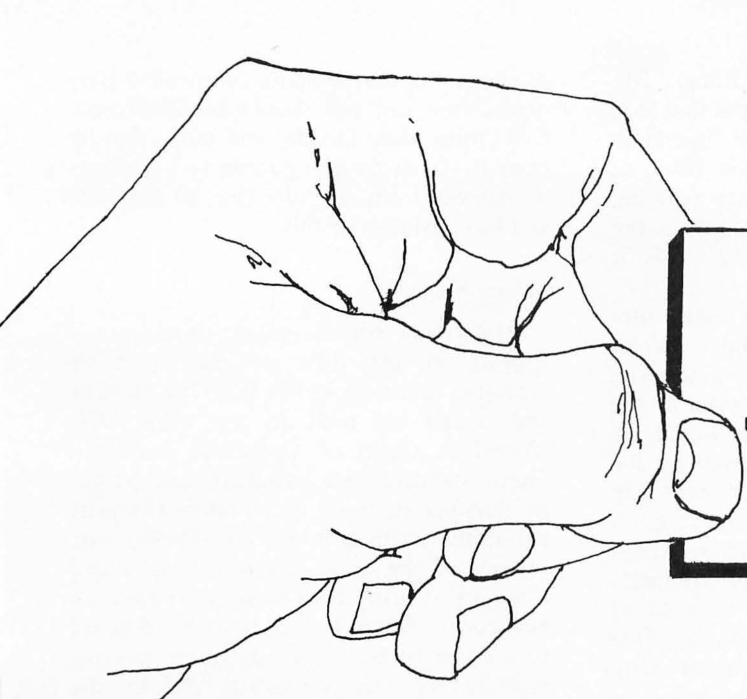
Another choice to be made is whether to recalculate all the pipes to be played, or just to modify the previous state on each cycle. It was decided to recalculate from scratch each time to eliminate the possibility of cumulative error. It also means that key bounce is automatically taken care of. In the slight time between updates, an organ pipe cannot even begin to sound. A spurious signal for one cycle is effectively ignored. Continuous pipe-on instructions emitted over a period of approximately 0.1 *second* or more are required before the slow mechanical valves can react. The higher pitched pipes respond quickly, incidentally, and the low pipes sometimes take nearly a second to begin playing. Organists learn to compensate by playing low notes somewhat early. Without introducing a constant across-the-board delay, it does not seem possible to have the computer compensate for the effect, but it is a place where some experimentation might be interesting. Experienced organists, of course, might look askance at such an innovation, but they needn't be told about *all* of our ideas.

To summarize: A cycle of the computer organ system starts by pulling in the state of the console. The second part of the cycle (yet to be described) calculates the pipes that should be playing, given the state of the console. The third portion of the cycle sends the pipe commands along the shift register. This process is repeated at least once every 1/30 of a second.

A coupler (of whatever kind) is merely a displacement. It is easily calculated because all keyboards and ranks are the same nominal length. Likewise, engaging a stop is also a displacement of a distance equal to the difference between the bottom of the manual's image in memory and the bottom of the rank's image in memory. Thus, these displacements or offsets can be simply added to yield the offset for a combined coupler-stop setting.

An example, with a simplified organ, will demonstrate how the algorithm operates. Say there is one manual with ten keys numbered one through ten. They are read into memory locations (all numbers will be in base 10 for this discussion) 1001 through 1010. The ranks each have ten pipes, and there are two of them. The first rank is stored in locations 2001 through 2030. The second rank is stored in locations 3001 through 3030. Remember that the area set aside for each rank is larger than the actual space necessary (here three times as large). There are two stop switches, stored in locations 4001 and 4002. There are two couplers. They are stored in 4003 and 4004. The first couples up five pipes high, the second down three pipes low.

When the low order bit in 4001 is on (or high), the program adds 2010 to the key address to get the pipe address. When the other stop is on, 3010 is added. If the first coupler is on, an *additional* 5 is added, and the second coupler subtracts 3 (or adds a



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This Editor has caused more talk than any other TSC program. Most users find it hard to believe its power. The TSC Text Editing System will allow extreme ease in any text preparation, whether it be an assembler language program or a legal document.

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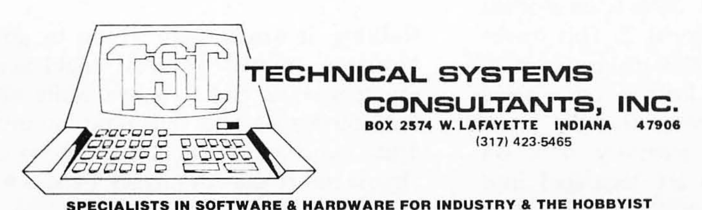
The Text Processor in conjunction with the Text Editor will give your micro the powers of the best text processing system available. The complete assembler language source listing and extensive users manual are included.

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8080

SL80-11	Manual and Source Listing	$32.00
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Circle 124 on inquiry card.

negative 3; it is all the same thing). The addition is done only once. Say the first stop and the second coupler were operated; then, given a key on at location 1005, to get the proper location to turn the pipe on, one merely adds (2010-3) or 2007 to the key location (1005+2007)=3012. This is indeed the correct pipe.

The microcomputer gives the user another option. When a stop and a coupler are operated, one gets both the note given by the stop and the extra note given by the coupler. With a computer it would be possible to give just the note given by the coupler acting on that stop. Since each stop can have a whole panoply of couplers attached to it, the number of buttons would soon become unworkable. For complete flexibility, the organist would have to be provided with a keyboard and display. One would play the organ by setting up many required presets with whatever degree of flexibility required, and then the easily hit tabs would not activate stops, but would bring in the organist's choice of registrations.

In the example above, choosing both stops and both couplers would necessitate the addition of six numbers to each key location to obtain the pipe location. In the actual implementation, the program would, for each manual, do the following:

1. Scan the list of stops, and make a table of addends.
2. Scan the couplers, and add them to each stop, extending the list of addends.
3. Add the addends to the locations of the manual that contain a 1 (meaning a key depression).
4. Turn on the low order bit in the indicated word in the pipe image.

Intermanual couplings look just like any other kind of coupling. Say that one manual is stored in 1001 through 1010, and another manual at 1201 through 1210. Coupling the first manual to the second merely means adding 200 to the locations of the first manual. Just which intermanual couplers will be allowed must be carefully specified. If anything is allowed, we may get the following cat chasing its tail effect: Manual 1 is coupled to manual 2 at the same pitch. Manual 2 is coupled to manual 1, but one key higher (a semitone or *half step* higher in musical terminology). Press C on manual 1. C gets played on manual 2. This forces C# on manual 1. But this makes C# play on manual 2. Every key is thus being played. As implied above, though, intermanual couplings are necessary only on organs where the pipes are separated into divisions. In the computer controlled pipe organ they can and should be eliminated. Everything they can do, and more, can be done by freely assigning ranks to keyboards as desired. I am not sure that all organists will be convinced by this.

Acknowledgements

Certainly at least half of the ideas expressed in this paper are due to my friend and colleague, Doug Wyatt. All of the ideas were developed in collaboration with him. Thanks are also due to Jim Brennan, who owns the incredibly large organ so often mentioned in and photographed with this article, and whose cooperation and inspiration have been essential to the project.

Future Fugues

The organ console of the future, as it appears in the light of the computer mediated organ, looks like this: The manuals and pedals are built to the usual AGO (American Guild of Organists) standards. These standards are excellent, and permit an organist to travel from one instrument to another with a minimum of relearning. Instead of the usual arrangement of stops, there are as many rows of stops as there are keyboards. When a stop is to be assigned to a given keyboard, the button in the row representing that keyboard, and in the column representing that stop, is pressed. Any particular registration may be captured by pressing the "capture" button and, while holding it, operating the chosen preset button. The stop buttons should, as on conventional organs, move (or light up) to show what choices have been made. This is not far from conventional practice.

The possibilities in a console screen, with alphanumeric readout, are endless, and would require another article to explore. Similarly, the gimmicks, from very useful ones that record (on a disk or cassette) the performance in terms of keystrokes, to silly ones (for example, connecting the doorbell to the computer, so that the organ plays "Jesu, Joy of Man's Desiring" when a visitor presses the door button) would again take up too much space here.

Summary

The reasons for using a computer in a pipe organ are these:

1. Simplification of the wiring of the organ.
2. Greater reliability than conventional switching.
3. Lowered expense in medium and large instruments.
4. Much greater control of the instrument by the performer.
5. New freedoms in choosing registrations.

Nothing, it would seem, is lost by going to a microcomputer, and one could keep advantages 1, 2 and 3 above while keeping the appearance and operation of the pipe organ unchanged, in case any organists choose not to use advantages 4 and 5.■

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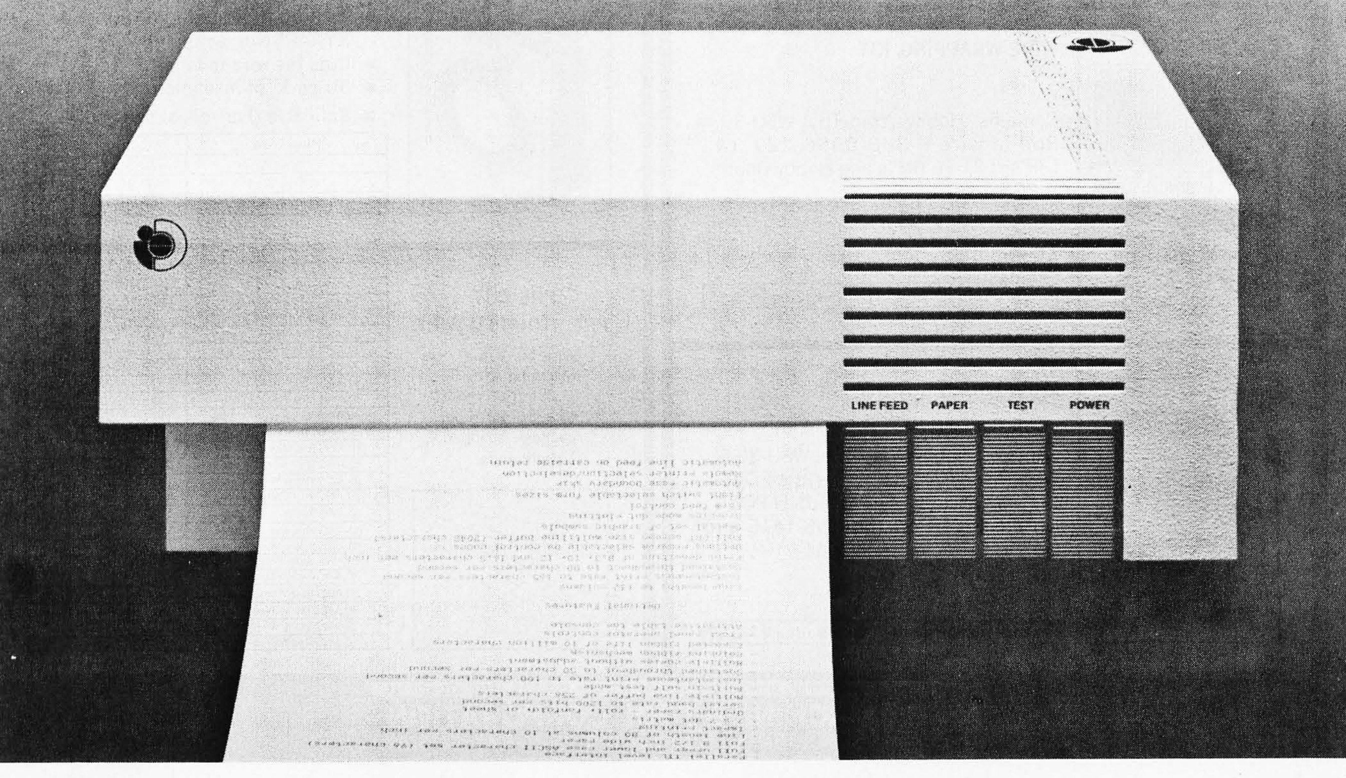
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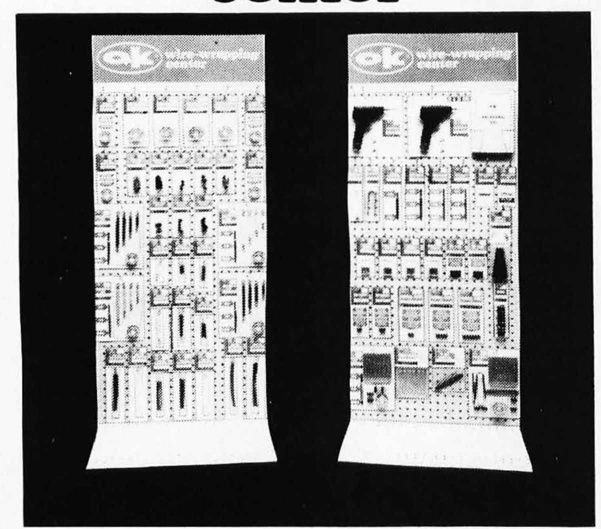
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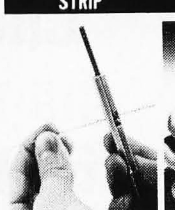


wire wrapping center



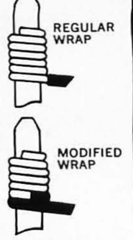
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STRIP WRAP UNWRAP









HOBBY WRAP TOOL

Wire-wrapping, stripping, unwrapping tool for AWG 30 on.025 (0,63mm) Square Post.

Regular Wrap	WSU-30	$6.95
Modified Wrap	WSU-30M	$7.95



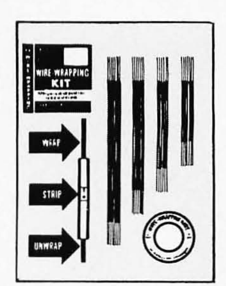
WIRE-WRAPPING TOOL

For .025" (0,63mm) sq. post "MODIFIED" wrap, positive indexing, anti-overwrapping device.

For AWG 30	BW-630	$34.95*
For AWG 26-28	BW-2628	$39.95*

Bit for AWG 30	BT-30	$3.95
Bit for AWG 26-28	BT-2628	$7.95

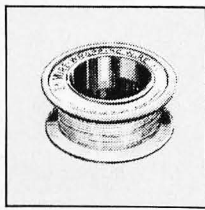
*USE "C" SIZE NI-CAD BATTERIES (NOT INCLUDED)



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Contains: Hobby Wrap Tool WSU-30, (50 ft.) Roll of wire Prestripped wire 1" to 4" lengths (50 wires per package) stripped 1" both ends.

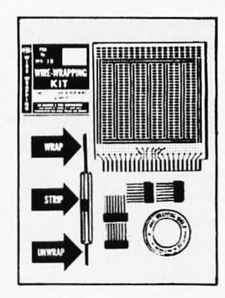
Wire Wrapping Kit, (Blue)	WK-2-B	$12.95
Wire Wrapping Kit, (Yellow)	WK-2-Y	$12.95
Wire Wrapping Kit, (White)	WK-2-W	$12.95
Wire Wrapping Kit (Red)	WK-2-R	$12.95



ROLLS OF WIRE

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30-AWG Yellow Wire 50ft. Roll	R-30Y-0050	$1.98
30-AWG White Wire, 50ft. Roll	R-30W-0050	$1.98
30-AWG Red Wire, 50ft. Roll	R-30R-0050	$1.98



WIRE-WRAPPING KIT

Contains: Hobby Wrap Tool WSU-30, Roll of wire R-30B-0050, (2) 14 DIP's, (2) 16 DIP's and Hobby Board H-PCB-1.

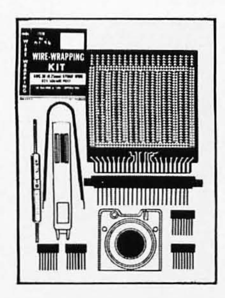
Wire-Wrapping Kit	WK-3B (Blue)	$16.95



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- With 50 ft. Roll of AWG 30 KYNAR® wire-wrapping wire.
- Cuts the wire to length.
- Strips 1" of insulation.
- Refillable (For refills, see above)

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Yellow Wire	WD-30-Y	$3.95
White Wire	WD-30-W	$3.95
Red Wire	WD-30-R	$3.95



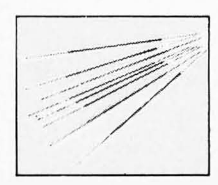
WIRE-WRAPPING KIT

Contains: Hobby Wrap Tool WSU-30 M, Wire Dispenser WD-30-B, (2) 14 DIP's, (2) 16 DIP's, Hobby Board H-PCB-1, DIP/IC Insertion Tool INS-1416 and DIP/IC Extractor Tool EX-1

Wire-Wrapping Kit	WK-4B (Blue)	$25.99

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30-AWG White Wire, 1" Long	30-W-50-010	$.99
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30-AWG Blue Wire, 2" Long	30-B-50-020	$1.07
30-AWG Yellow Wire, 2" Long	30-Y-50-020	$1.07
30-AWG White Wire, 2" Long	30-W-50-020	$1.07
30-AWG Red Wire, 2" Long	30-R-50-020	$1.07
30-AWG Blue Wire, 3" Long	30-B-50-030	$1.16
30-AWG Yellow Wire, 3" Long	30-Y-50-030	$1.16
30-AWG White Wire, 3" Long	30-W-50-030	$1.16
30-AWG Red Wire, 3" Long	30-R-50-030	$1.16
30-AWG Blue Wire, 4" Long	30-B-50-040	$1.23
30-AWG Yellow Wire, 4" Long	30-Y-50-040	$1.23
30-AWG White Wire, 4" Long	30-W-50-040	$1.23
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30-AWG White Wire, 5" Long	30-W-50-050	$1.30
30-AWG Red Wire, 5" Long	30-R-50-050	$1.30
30-AWG Blue Wire, 6" Long	30-B-50-060	$1.38
30-AWG Yellow Wire, 6" Long	30-Y-50-060	$1.38
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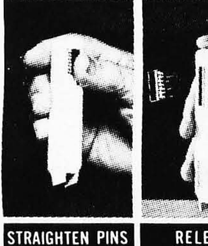
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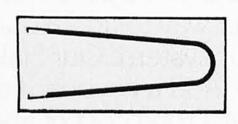





STRAIGHTEN PINS | RELEASE | PICK-UP | INSERT

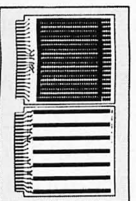
14-16 Pin Dip IC Inserter	INS-1416	$3.49

DIP/IC EXTRACTOR TOOL



Extractor Tool	EX-1	$1.49

P.C. BOARD

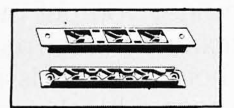
The 4 x 4.5 x 1/16 inch board is made of glass coated EPOXY Laminate and features solder coated 1 oz. copper pads. The board has provision for a 22/44 two sided edge connector, with contacts on standard .156 spacing. Edge contacts are non-dedicated for maximum flexibility.

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Two independent bus systems are provided for voltage and ground on both sides of the board. In addition, the component side contains 14 individual busses running the full length of the board for complete wiring flexibility. These busses enable access from edge contacts to distant components. These busses can also serve to augment the voltage or ground busses, and may be cut to length for particular applications.

Hobby Board	H-PCB-1	$4.99

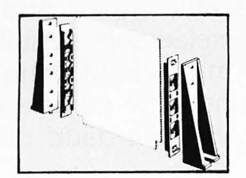
PC CARD GUIDES



Card Guides	TR-1	$1.89

QUANTITY — ONE PAIR (2 pcs.)

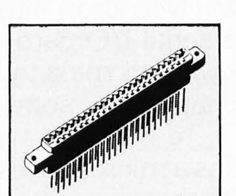
PC CARD GUIDES & BRACKETS



Guides & Brackets	TRS-2	$3.79

QUANTITY — ONE SET (4 pcs.)

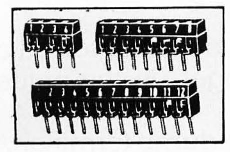
PC EDGE CONNECTOR



44 Pin, dual read out, .156" (3,96 mm) Contact Spacing, .025" (0,63 mm) square wire-wrapping pins.

P.C.. Edge Connector	CON-1	$3.49

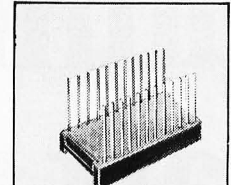
P.C.B. TERMINAL STRIPS



The TS strips provide positive screw activated clamping action, accommodate wire sizes 14-30 AWG (1, 8-0, 25mm). Pins are solder plated copper, .042 inch (1mm) diameter, on .200 incn (5mm) centers.

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8-Pole	TS- 8	$1.89
12-Pole	TS-12	$2.59

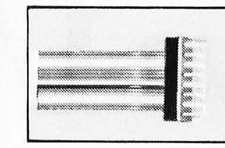
DIP SOCKET



Dual-in-line package, 3 level wire-wrapping, phosphor bronze contact, gold plated pins .025 (0,63mm) sq., .100 (2,54mm) center spacing.

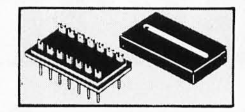
14 Pin Dip Socket	14 Dip	$0.79
16 Pin Dip Socket	16 Dip	$0.89

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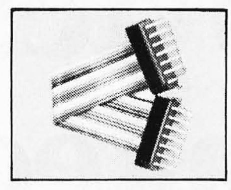
DIP PLUG WITH COVER FOR USE WITH RIBBON CABLE



14 Pin Plug & Cover	14-PLG	$1.45
16 Pin Plug & Cover	16-PLG	$1.59

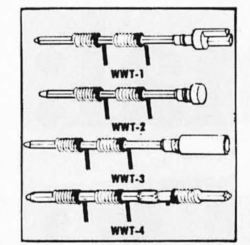
QUANTITY: 2 PLUGS, 2 COVERS

RIBBON CABLE ASSEMBLY DOUBLE ENDED



With 14 Pin Dip Plug - 2" Long	DE 14-2	$3.75
With 14 Pin Dip Plug - 4" Long	DE 14-4	$3.85
With 14 Pin Dip Plug - 8" Long	DE 14-8	$3.95
With 16 Pin Dip Plug - 2" Long	DE 16-2	$4.15
With 16 Pin Dip Plug - 4" Long	DE 16-4	$4.25
With 16 Pin Dip Plug - 8" Long	DE 16-8	$4.35

TERMINALS

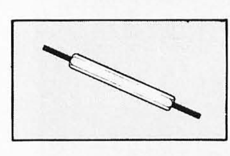


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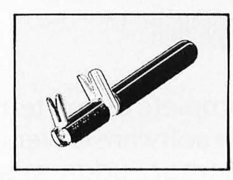
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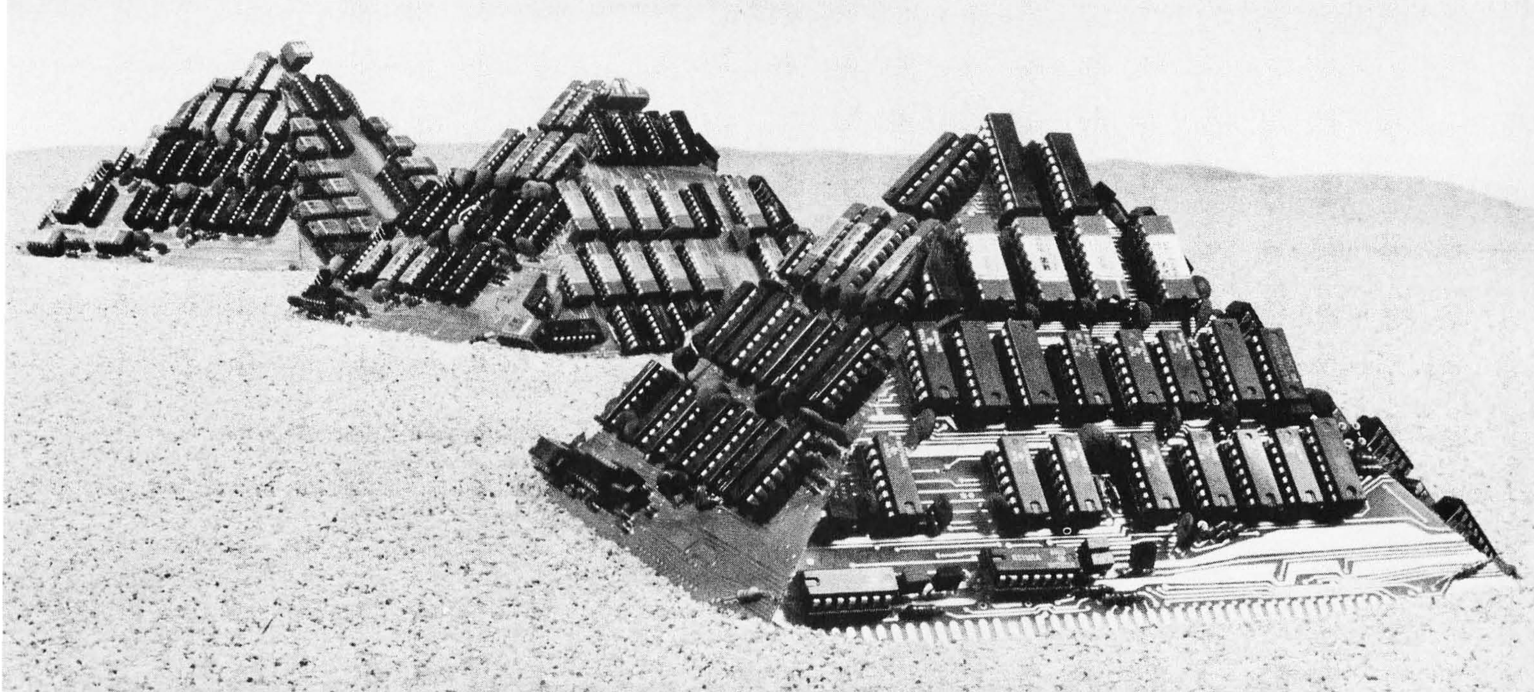
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Ernest W Kent, Associate Professor
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The Brains of Men and Machines

Part 3: How the Brain Analyzes Input

Note: *A number of the terms which are used in this article were defined and discussed in the first article of this series which appeared in Janurary 1978 BYTE, page 11.*

Perhaps the most remarkable feat performed by organic brains is the resolution of the flood of data flowing from the sensory receptors into conceptually meaningful elements. It is also one of the most difficult tasks faced by the designer of robot systems. Consider the nature of the information which the brain receives about the visual world. Patterns of light, of varying wavelength and intensity, are imaged on the retina of the eye by the lens. This illumination results in a barrage of neural impulses flowing through millions of fibers in the optic nerve and activating neurons in a portion of the cerebral cortex called the primary visual cortex. Obviously, our visual *experience* is nothing like this barrage of impulses in axons. We "see" objects, colors, groupings of objects, all interpreted in meaningful terms. Our experience of the visual world is thus a far different matter from the visual stimulus which initiates the experience. It is not necessary that a robot have "experience" as we do, but it is necessary for one to resolve the sensory information into behaviorally relevant elements as we do.

To understand the nature of the operations that are being performed, we must carefully discriminate between the terms "stimulus" and "sensation." "Stimulus" refers to the actual physical event that activates a receptor. In the case of vision, this would be a ray of light falling on the retina. Since the intensity and wavelength of this light are determined by properties of the physical object which reflects it, and since there is a fixed relation between the two, we often refer to the reflecting object as the stimulus, with the understanding that its action as a stimulus depends on the properties of the light it reflects. "Sensation" on the other hand refers to a property of our mental experience which results from certain kinds of activation of our receptors. There is a close relation between the sensations we have and the stimuli which produce them. Our senses would be useless if it were not so. However, this close relation often leads us to confuse the two, and this is a great error, because they belong to entirely different worlds. A stimulus is a physical object; a sensation is a mental event.

To clarify the distinction, consider the sensation of the color red. We all know what we mean when we say an object "is red," or that we "see a red object." A moment's reflection though will demonstrate that, strictly speaking, there can be no such thing as a red object. The object can only possess or not possess the properties necessary to reflect light of a particular wavelength. If an

object reflected light of a wavelength which gave rise to the sensation "red," and we were to somehow change the wavelength between the object and the eye, the object would appear to be of some other color. Can we then say that "redness" is a property of the light? No, because the only relevant physical property of the light is its wavelength, and wavelength is not a color. Color is a property of your sensation.

Sounds have wavelengths too, and there the sensation is interpreted as pitch. Wavelength is only a piece of information which the brain can interpret as it will. In your computer, you could make an analogy with ASCII code. We use particular bit patterns to represent letters and numbers, but the same bit patterns could just as easily represent something else. There is nothing that inherently requires the binary pattern 01000001 to be interpreted as A. Similarly, "redness" as an interpretation of a particular wavelength is simply a convention that the brain uses.

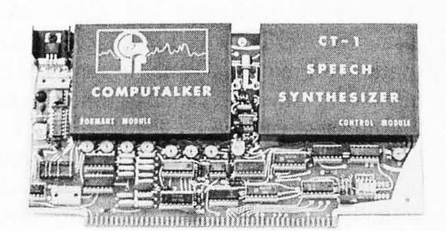
The situation becomes clearer if one goes into the brain a little further. Sensation is not a result of activating the retina or the optic nerve. If the optic nerve is cut, light falling on the retina produces no sensation, even though the retinal neurons and their axons in the optic nerve are activated. At the same time, however, artificially activating the visual cortex to which the nerve used to project will result in visual sensations. It follows that sensation is, or is dependent upon, the firing of neurons in the visual cortex. Yet, after striking the retina, light never reaches the visual cortex. All that does reach it is a pattern of neural activity in the axons of the retinal cells. Information about the wavelength of the light striking the retina is carried in the optic nerve by place code. That is, the wavelength information is carried to the visual cortex in terms of *which* lines are active. There is certainly nothing that seems intuitively "red" about which of a set of axons are carrying impulses. Yet, the sensation of "redness" clearly occurs at or beyond the cortex, *after* that encoding process. If we could somehow change which set of axons were active between the retina and the cortex, the sensation produced by the light would change.

Sensation ≡ Information Processing

Now if we accept the notion that sensations are mental events that are produced, or

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at least determined, by the brain decoding stimulus produced activations of receptor lines according to specified conventions, it becomes clear that the process of sensation is basically one of information processing. The nature of the conscious "experience" of the processed data is a topic we shall take up later. For now, our objective will be to examine the kinds of transformations the brain imposes on its input data and to ask why this particular transformation and not some other is useful to the organism in dealing with the environment. The utility of such a pursuit lies in the fact that the most likely system for detailed examination of distant objects in an artificial robotic system will use an image forming system acting on a grid of sensitive transducers. The problems of information processing in such a system will be exactly those that the brain has solved.

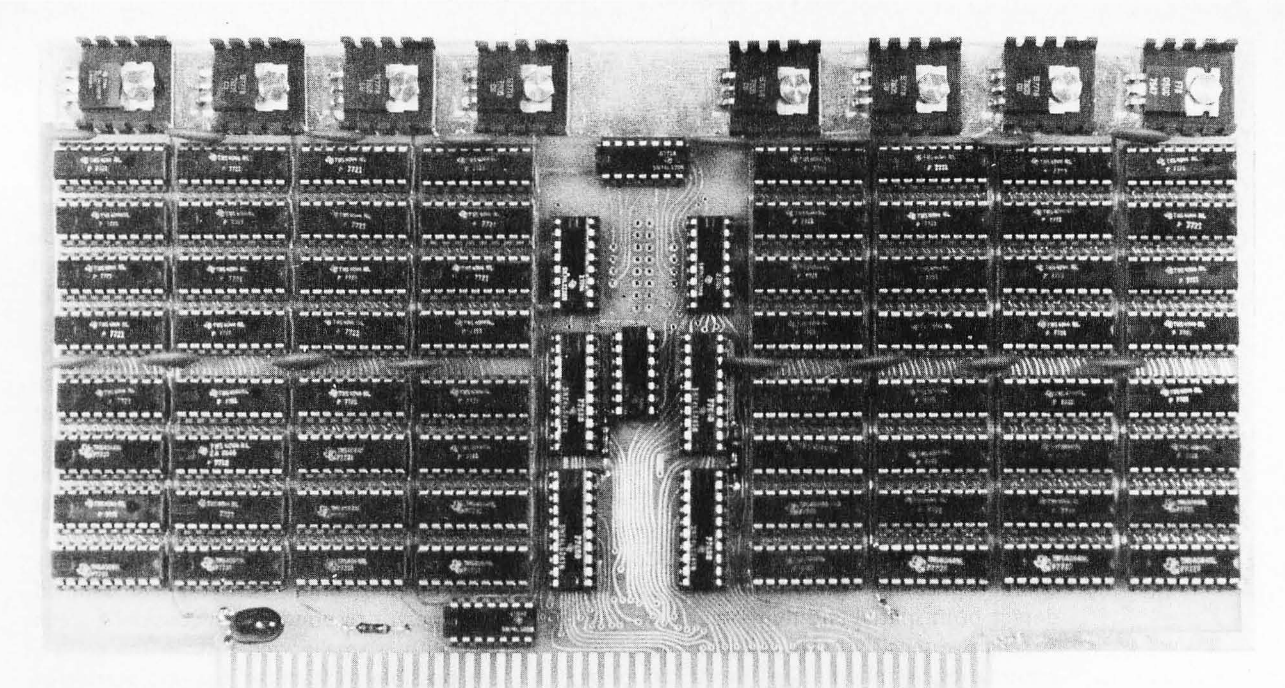
There are about a million light receptive elements in the retina, and the brain produces a complete analysis of their patterns of illumination about ten times per second. If this were done in a straightforward manner, say by examining all the possible permutations of a million bits of information and decoding it against a table of known codes, a tenth of a second's worth of vision would be too big a job even for the brain to handle in a reasonable time. In fact, it goes to some extremes to cut corners in this process, and some of its tricks are of quite general utility. The first step in the process is to make a number of decisions about what not to look at.

If an area of uniform illumination is bounded by an area of some other degree of illumination, the information from the center of the area is superfluous. That is, if one had a system that could detect only boundaries between different illumination levels, the center of a uniform bounded area would not produce a signal. Yet, information about its illumination could be accurately reconstructed by simply extrapolating the illumination level on the inside edge of the boundary clear across to the next boundary. If the level at the inside edge of the boundary did not hold clear across the area, that would mean that there had to be a change, and hence a boundary, somewhere in the middle, and that boundary would be detected. Any *change* in illumination constitutes a boundary between a lighter and a darker region. Thus, if only boundaries can be detected, extrapolation of levels on either edge of a boundary to the next boundary reconstructs the whole field of illumination.

The reduction in the number of points to be considered which is achieved by considering only boundaries is quite large. Think of a square patch of retina 100 receptor cells on an edge, illuminated at level A on the right half, and level B on the left. If we had to examine every element's illumination to arrive at a picture of this pattern, we would have to examine 10,000 elements. If we now examine only the ones near the boundary between area A and area B, and extrapolate the rest, we have to examine only about 100 elements. In general, the savings go up approximately as the square of the boundary of a uniform area.

We will return in a moment to the matter of how the brain locates spatial boundaries, but first mention should be made of the next shortcut, because their underlying mechanisms are related. Basically, this second trick is to look only at things that change. Aside from the fact that changing patterns of illumination usually imply moving objects, and that these are usually important items in the sensory world, special attention to change also has advantages in terms of processing time. The situation is really very similar to the preceding one, except that here we must think of change as representing a *temporal* boundary between illumination levels. If we only attend to an element when its illumination changes, and if we always know when it does, we can safely ignore it in the meantime. This is because the illumination during the intervening period of no change must be at whatever level the preceding change brought it to. Thus, it is only necessary to extrapolate the value immediately following a change until the next change is detected.

The eye is sensitive to two dimensions of light, intensity and wavelength, which we perceive as brightness and color. We have discussed the two boundary situations, spatial and temporal, only in terms of brightness so far, but the same arguments apply to boundaries of color. Two areas of equal brightness but different color also must be discriminated. The same mechanisms actually are applicable to both, since the brain handles color by providing some receptor elements with differential sensitivity to different wavelengths. For these elements, a change in wavelength effectively *is* a change in illumination. It will either be from a wavelength to which the element is sensitive to one to which it is not, or *vice versa*. The brain handles the color information simply by recognizing the output of these elements as encoding the wavelength information, and interprets it as color. The color



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boundary problem therefore reduces to the intensity boundary problem.

Now let us examine the mechanisms of boundary detection. The temporal boundaries, that is, changes in illumination with time, are responded to selectively by a process that is similar in its results to AC coupling the receptor elements. In fact, AC coupling of analog to digital converters with an appropriate time constant would be a good way to model the process in a robot. In the brain, it is simply a property of the receptor neurons themselves, and the details need not concern us. The interesting thing is that the brain uses this same AC coupled characteristic of the neural elements to detect both spatial and temporal boundaries. A selective sensitivity to change, or temporal boundaries, is inherent in the AC coupling, but a sensitivity to spatial boundaries requires some additional mechanism.

We are all aware of course that the eye moves. We observe it all the time when our gaze turns from one point of fixation to another, or when it follows a moving target. In addition to these motions, however, there is another that is not detectable by ordinary means. Even when the eye seems to be at rest, even when you are holding your gaze as intently as possible on a fixed point, there is still a very fine motion with a frequency of about 10 Hz. The amplitude of this motion, which is rather erratic in its direction, is just sufficient to move the retinal image back and forth over the receptors by a distance equal to a few times the average separation between the sensitive elements. Those elements that are near a boundary are thus swept back and forth continuously from the lighter to darker sides of the boundary at about 10 Hz. This produces in them a changing signal of the sort to which the AC coupled property of the system can respond. At the same time, their neighbors further from the boundary in either the lighter or darker regions to either side are not moved into a region of different illumination level. Hence, they "see" an unchanging input, to which they are insensitive. The receptor elements of the eye itself therefore act as intelligent terminals which transmit only information about boundaries and changes to the higher levels, with an enormous savings in amount of input requiring attention from more sophisticated analyzers.

Now I hear you say, "Yes, but I can see the insides of uniform areas." True, but remember I said your sensations were an arbitrary decoding of the stimulus information, and that the information from areas distant from boundaries was redundant and could be reconstructed by inference or extrapolation. The experience of "seeing" the inside of the area is simply the experience of receiving the appropriate code from the right set of boundary activated elements. In the first place, it is relatively easy to demonstrate that you cannot see anything if there is no change. By virtue of some clever optics it is possible to stabilize an image on the retina so that it does not move with respect to the receptor elements, despite the fine motions of the eye. When this is done, the image seems to disappear about a tenth of a second after it is presented: poof! It is of course still really there on the retina, but your AC coupled system can't respond. Now, consider a green disk with a smaller red disk in the center. It is possible to stabilize just one portion of this image in the same fashion that we stabilized the whole image a moment ago. If we choose to stabilize just the boundary between the green outer ring and the red inner disk, it should not be possible for the brain to detect that boundary. If this is done, not only do you not see the boundary, you also don't see the inner red disk. What do you see? You see an unbroken green disk all the way across. In other words, if no boundary is detected in the middle, the brain not only doesn't see the red disk, it extrapolates the green all the way across from one outer boundary to the other. Think about it the next time you rely on the evidence of your eyes: such evidence must be interpreted with *knowledge of the* system's characteristics.

The AC coupling is not perfect; there is a "DC leak" around it, but the "changing signal only" property of the neurons is enhanced at each step in the transmission process, until the cells of the visual cortex are found to have almost no response at all to unchanging uniform illumination of the retina. This means that the sensory experience of the interiors of uniform regions is simply what is coded for at the cortex by the byte of information on the boundary conditions. It is not a result of direct translation of retinal illumination conditions on a point for point basis into activation of some set of "experience neurons." It is important to grasp this idea, because it points up the fundamental similarity between the natural brain and the artificial computer. There is no "inner eye" looking out through neural windows. If the encoding process ultimately produces a single neural line that is activated by, say, the sight of a face, then that line being active is sufficient for the processing of response to the face, in man or robot; and at least in us,

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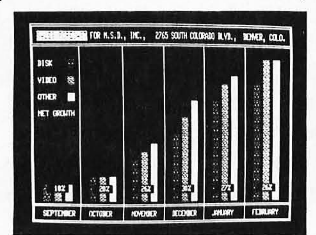
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it is also sufficient for our correlated mental experience.

That this is the nature of the encoding process for our experiences becomes even clearer at higher levels of the encoding process than those involved in the green and red disk experiment. At some level of the process, referred to as "feature extraction," we arrive at a byte of active lines which encodes for some complex pattern. Take for example the repeated patterns of a wallpaper covered wall. It seems that even at this level, the brain continues its policy of dropping redundant information and carrying forward only information on boundaries. If we look at such a wall, we of course see a continuous pattern repeated all the way to pattern boundaries such as the ceiling floor, edges of intervening furniture, etc. Now suppose we present this same scene to a person with damage to certain high levels of the visual system, having no vision in a particular small region of the visual field. If his injury is at the right level in the feature extracting process, he will report seeing the unbroken wallpaper pattern just as we do, including the region within which he is "blind." It can be demonstrated, however, that his experience of the pattern in the blind region is due to the fact that both he and we are extrapolating the detected pattern across the intervening space between pattern boundaries. His deficit becomes apparent when we create a boundary in the pattern within his blind region. For example, if we inverted a small patch of the pattern, it would constitute a boundary in the pattern, and we would not extrapolate across it. If it occurred in his blind region, however, he would not react to the pattern boundary and would receive the same encoded byte of visual information as before, and claim that he saw an unbroken wallpaper pattern. In an important sense he is blind, yet he has visual experience. You do the same thing. There is a blind spot in the visual field where the optic nerve leaves the retina. You can make small objects disappear by centering them there, but since you can't see boundaries there either, your brain normally extrapolates across it.

Now we might ask, if the brain is reducing complex features of the visual stimulus to a simple code of one or a few lines, does that mean there are things we might not have feature extractors for, and if so, would we be unable to see them? That is probably exactly the case. Experiments suggest that the visual world of simple creatures like frogs is quite impoverished. They have some kinds of elementary feature extractors, and some complex ones for stimuli (eg: bugs) which are important to their behavior, but nowhere near the complex set of feature extractors that a mammal has. In theory it would be possible to have a unique line or coded set of lines activated by every possible combination of activities on the retina, but this would be beyond even the capacity of the nervous system to generate processing elements. Instead, certain decisions are made as to what things are important to see, and decoding for these is provided. This does not imply that you would not see anything when looking at a novel stimulus for which you have no appropriate high level extractors. At the first level, simple features such as edges, arcs, lines and spots are extracted. More complex features are extracted from combinations of these. You might be aware only of the activity of the low level extractors for lines, edges, etc, and fail to recognize it as an object, or you might fail to discriminate it from objects which were not identical, but differed in ways which did not correspond to features you could extract.

As an example, it is possible to fool high level extractors by giving them marginal data. Look at figure 1. About 95 percent of people seeing this picture for the *first time* are only able to activate low level extractors for patches of bounded light and dark. It is in fact a photograph of the head and upper forequarters of a black and white cow (facing left) against some trees and a fence. Once you know what to look for, you can nudge the "cow extractors" and get an entirely different experience. Indeed, once you've seen it, it's difficult to not see it. (Don't panic if you can't; about 5 percent of people never see it.)

Actually, there is probably no "cow extractor" per se, but rather some assemblage of feature extractors which together constitute a code for "cow." Let's look however at some of the properties which such high level extractors should have. The most important one is that they should be free of constraints on position, orientation, context, etc. That is, if we had to have a separate extractor for every position the stimulus might assume in the visual field, we would need so many elements that the advantages of the feature extractor approach would be lost. Next, they should be capable of implementation by learning, so that the available processing elements can be best used to fit the organism's normal visual environment. Third, they should not be limited to spatial forms, but should include detectors for properties such as motion, distance, and other aspects of our visual



experience. These are difficult problems, and we have no good notion of the real number or nature of the highest order extractors in the human visual system. We can examine some of their properties by fatiguing the extractors through prolonged exposure to different types of stimuli and looking at the effects on our visual abilities. In animals, we can follow the process by recording activites of neurons in the visual system during presentation of stimuli to the eye.

From these latter experiments, we have a fairly clear notion of the operation of the lower order extractors, and the process seems easily extensible to higher order features. To serve as a general example of the algorithm, I will describe in detail the process by which a feature extractor is formed which can detect a line segment only if it is at a particular angle of inclination to the visual field, but which is location independent. That is, it does not matter where the line is located in the visual field, only that it be a line and that it possess a certain angle of inclination. This sort of unit appears to be one of the typical low level feature extractors of mammalian visual systems.

The basic gating action used is very similar to an AND gate. As we have mentioned, this is one possible mode of action of neurons, which can be implemented by hav-

Figure 1: A white cow with black ears and nose. The head is turned facing you, with the side of the head in shadow. The large white area in the lower right is part of the cow's left flank. Before you "see" the cow, all that appears are white and dark areas. After you "see" the cow, your sensory experience is still the same in terms of the stimuli you are receiving, but your analysis is very different.

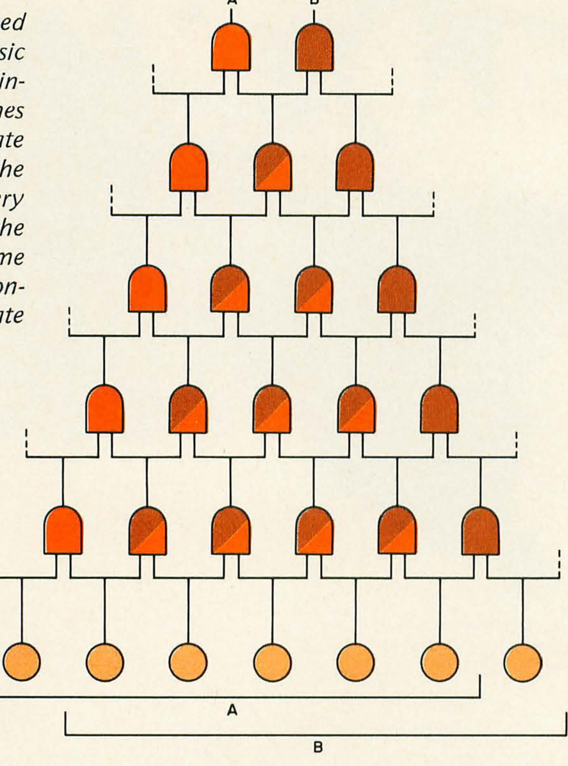


Figure 2: The generalized case of the brain's basic approach to processing input. The two output lines at the top discriminate patterns of input at the bottom that are very similar. In reality, the brain chooses only some of these possible connections to facilitate processing.

ing a number of inputs required to achieve firing threshold. In this case, however, we have an AND gate with a safety factor. By this I mean that firing level is achieved if some percentage of the relevant inputs are active: 100 percent is not required. Think of it as an "ALMOST gate." (The brain, unlike our conventional computers, is continually dealing in "best guesses" rather than precise solutions, by just this technique. This is why we make mistakes, but it also provides for inductive leaps of enormous power that are right most of the time.) Connecting a grid of two legged AND gates together, as in figure 2, illustrates the basic logic of the scheme. At the bottom level we have a line of receptors. Above these are several levels of two legged AND gates, culminating in the top level with only two elements. It is clear that the two top level elements will discriminate between two patterns of activation of the bottom row which differ only by one element. Thus, activation of element A encodes the activity of a set of bottom level elements indicated by bracket A, and element B and bracket B represent a different set. If the bottom row were retinal receptor elements, A and B could be feature extractors for illumination conditions (A) and (B), which are quite similar. It should be apparent that with enough gates and elements, this sort of general convergence scheme could be employed to extract any feature. This being impractical, the brain adds two principles which enormously reduce the processing required, at the expense of generality. Once the set of retinal activation patterns to be recognized has been selected, specific feature extractors for that pattern are built from the underlying type of logic illustrated in figure 2, but modified by the addition of processes called "selective convergence" and "lateral inhibition." The meaning of these terms will become clear shortly. At the lowest levels, only a few simple types of feature extractors are implemented and higher levels build progressively on these. To begin with, let us examine the first step in this process.

Within the retina itself, there are several levels of processing resulting in an output neuron, a retinal ganglion cell (RGC), which sends its axon into the optic nerve to enter the brain. If we record from these RGC neurons, we find that they can be classified into a few basic types depending on the kinds of stimulus to which they maximally respond. Figure 3 shows the portions of the visual field which affect the activity of a typical RGC type, and figure 4 shows the connections which result in this type of response. We see that the RGC receives positive synapses from a small group of receptor elements located in a central spot (+ region), and inhibitory synapses from receptor elements in a ring surrounding this spot (– region). Remember that the type of synaptic effect is the choice of the receiving neuron, the receptor elements in the "inhibitory surround" area are free to make

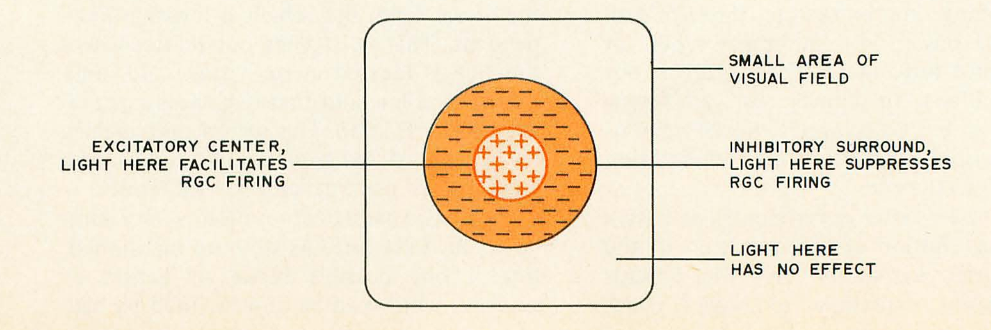


Figure 3: A small area of the visual field, showing the portions which can influence the output of a single retinal ganglion cell (RGC) when illuminated. Some visual neurons act inhibitory (–), others act excitatory (+).

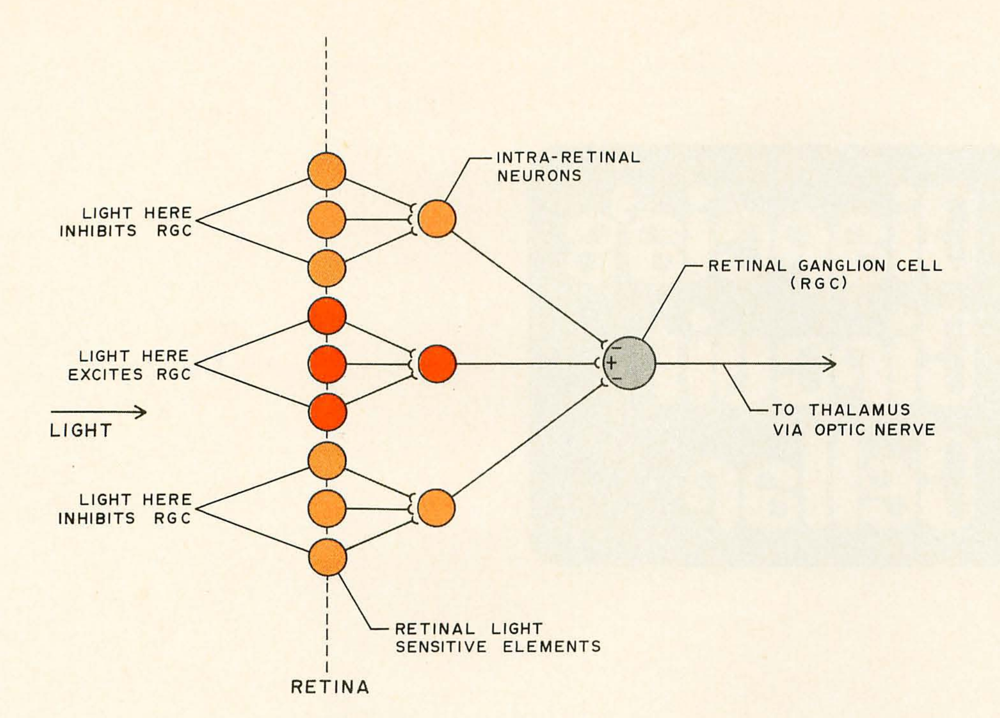


Figure 4: The connections between the retinal elements and the retinal ganglion cell (RGC) which account for the pattern of sensitivity shown in figure 3. In this view, the pattern of figure 3 would be edge-on as projected on the retina.

facilitatory positive connections with other RGCs. Now, when the central spot receives light, it increases the firing rate of the RGC. When the inhibitory surround is illuminated, it decreases the firing rate of the RGC. (In this and all subsequent descriptions, it is to be taken as understood that we refer to the intermittent presentation of the stimulus, either deliberately or through fine motion of the eye, since the AC coupling properties would tend to eliminate the response to any maintained stimulus.) If the entire retinal area which affects our RGC is illuminated, the excitatory and inhibitory effects tend to cancel. Here as elsewhere in the visual system, there is thus little response to diffuse light. Notice that due to the shape of the inhibitory and excitatory regions, a line of light just the width of the excitatory center spot, and crossing the entire active area, would fire retinal elements in both the inhibitory and excitatory regions. However, such a stimulus would fire the entire excitatory central region, but would only fire a small percentage of the inhibitory elements since it only crosses the inhibitory ring in two spots (see figure 5). The response to a line stimulus crossing the central spot would therefore be strongly positive, although less so than to a stimulus which did not touch the inhibitory region.

There are several other basic types of RGC organization with regard to the sizes and shapes of the retinal areas whose illumination affects them. For example, another common type has the inverse of the type of receptive field just considered, that is, an inhibitory center area surrounded by an excitatory ring. We shall not pursue these in detail, but pass on further into the brain with the development of our abstracted inclined line detector. The next way station, the target of the optic nerve, is a nucleus of the thalamus, called the "lateral geniculate nucleus." The axons of the RGCs make synaptic contact with the cells of this nucleus just as the retinal elements made contact with the RGCs. If we record from these cells while testing for retinal areas that excite or inhibit them, we find that

Continued on page 94

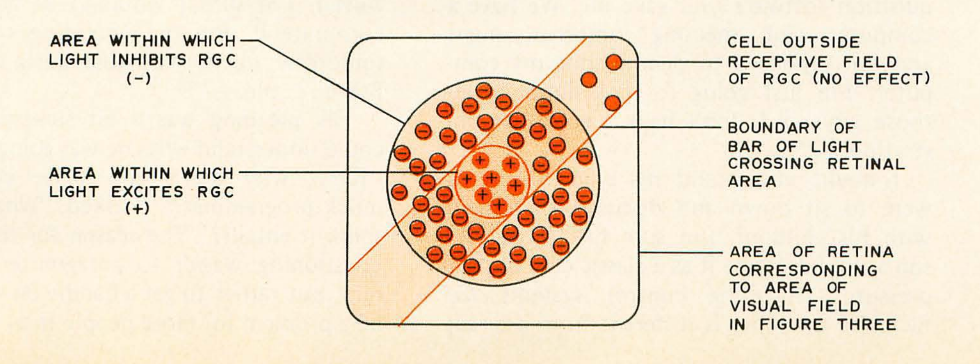


Figure 5: An area of the retina corresponding to the area of the visual field in figure 3, showing the retinal elements of figure 4 which would be activated by a stimulus consisting of a long line of light.

Ciarcia's Circuit Cellar

Program Your Next EROM in BASIC

Steve Ciarcia
POB 582
Glastonbury CT 06033

"Steve, you just gotta help me!" was my not so usual frantic midafternoon introduction to Jerry. He burst into my office with a manner reminiscent of a storm trooper. The vacuum he created as he rushed toward me around the obstacles in his path caused disturbed paper work to flutter slowly to the floor in his wake. He stopped abruptly at my desk and held the contents of his hand under my nose, hoping to exact an immediate response from me. Being abruptly summoned and having objects stuffed in my face is not generally how I like to be approached.

"I hope I'm not disturbing you, Steve, but I need some help." He extended his hand again but knew enough not to stick it in my face. "I accidently blew one of the EROM chips that contains the data acquisition software you gave me. We have a computer club meeting tomorrow night and I'm supposed to demonstrate my computer. I'm just going to look dumb to all those guys if I don't have a good demonstration. . ."

I could understand his plight. If Jerry were to sit down and discuss his problem with his children, I'm sure his 9 year old son would describe it as a classic case of peer pressure. Designing control systems for factories on paper is different from a direct demonstration of one's capabilities in front of a knowledgeable group of fellow computerists. Jerry was terrified that he would be a flop.

"Hold it Jerry... what's the problem? You have a computer... I thought you bought an EROM programmer?" I asked, still trying to ascertain the true depth of his difficulty. "You have a listing of the EROM contents."

"I've been meaning to get a programmer one of these days, but it costs a fortune. I wouldn't use it enough to justify the expense. I called Bob and he let me look at the assembly listing of an EROM programmer. I brought it along so we could cut another on your system. I've never been very good at assembly language programming. The listing of his programmer looks quite involved. I'm sure I wouldn't be able to incorporate it into my operating system by tomorrow night. You just gotta help me, Steve . . . please?"

His pleading was a bit sickening but I could understand what he was going through. "Jerry, why don't you write your own quick programmer?" I asked. "What do you think it entails?" The reason for this line of questioning wasn't to antagonize or delay him, but rather to get a handle on what may be a problem for more people than Jerry.

"What do you mean? How to do it? You write an assembly language program that gets the address and data to the EROM and you hold it there until it's burned in, and step to the next address. But it's all those program loops to keep track of the address, data and timing. I really bought this computer to use on BASIC, remember?"

"You've done some extensive BASIC programming, haven't you? You have a computer with plenty of parallel input and output ports, don't you? Write the EROM programmer in the language you understand best. True, it can be written in assembly language, but it can just as well be written in BASIC."

"Huh?" he grunted, still not quite believing me. "What do you mean?"

I felt I had his interest now. I was telling him that solving his dilemma need not entail using any more than the canned software supplied with his system, and that he didn't have to get involved with the "black magic" of assembly language.

"You already said that programming an EROM entailed getting the address and data to the EROM and stepping the address sequentially. Right?" I said.

"Yes, but BASIC?" he responded.

"Sure, why not BASIC?" I said. "By using INP and OUT commands, address and data can be set, and PEEK and POKE commands allow the interface data to be read into or from memory." It was important to convince him of the true value of high level languages. "You have a monitor program resident in your system that could allow you to just key the EROM data list into memory somewhere, don't you?"

"Yes, but . . . ."

"No buts! Just write a BASIC program that transfers this memory table one byte at a time to the read only memory." I felt I was really on the move now; I was going to "learn" him something if it killed him.

"Yes, but my BASIC is an interpreter. It runs pretty slowly. It's no match for an assembly language program. Assembly language loaders can program an EROM in 100 seconds; BASIC would be an order of magnitude. . . ." It was necessary to interrupt him at this point. Jerry was caught up in the old argument of potential versus accomplishment.

"Jerry, except for the time taken for data entry and printing, how long do your average BASIC programs run?"

"Oh, 5 or 10 minutes I suppose; why?" Jerry was not so curious that he had forgotten his problem, but his responses had become less acidic.

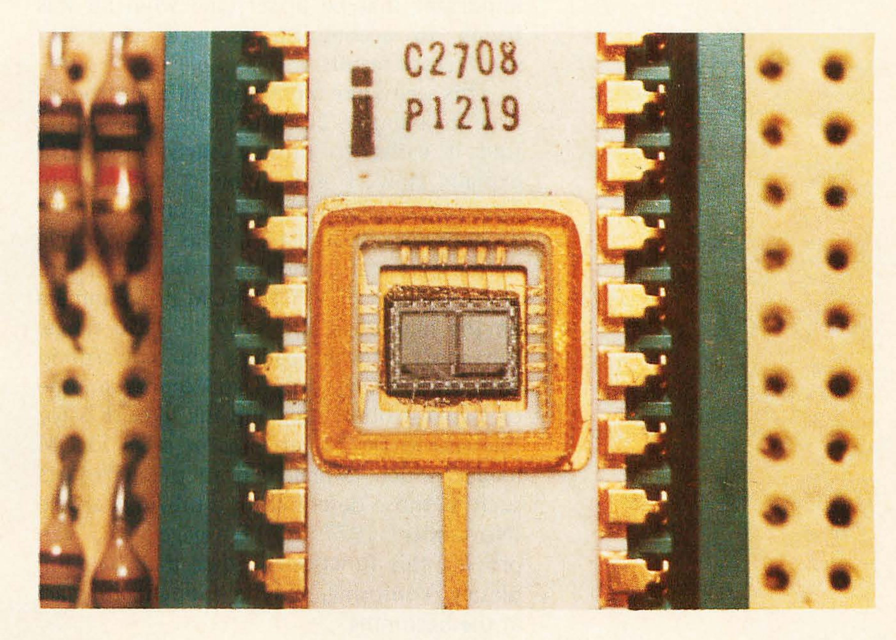


Photo 1: A closeup of a 2708 erasable read only memory. Visible through the transparent quartz window are the two banks of FAMOS (Floating gate Avalanche injection Metal Oxide Semiconductor) storage devices. The contents of this memory storage circuit are erased by exposing the window to ultraviolet light.

"And what do you do in between program runs or when you go upstairs for supper?" As oblique as my question may have seemed, I was driving to a point.

"I leave the computer on, of course, so I don't have to reload the BASIC. Everybody does that. Don't you?" His response was reminiscent of a child not sure whether he would be reprimanded for raiding the cookie jar or not telling that he raided the cookie jar.

"Jerry, what you just said is that if no operator interaction is required with the computer, execution time is irrelevant. Furthermore, if you started a program like an EROM loader on off peak use periods, you couldn't care less if it took a minute or an hour to run."

"Yes. . .but. . . well, I guess you're right." He had apparently never thought to use BASIC.

"In conclusion, Jerry, what language are you best able to program?" I had to be careful I didn't come across too strongly, but it was never too late to learn.

"BASIC, of course. I know how to program in assembly language, but. . .," he continued, still believing that there was something wrong about taking a different approach to the accepted norm.

"Then program the bloody EROM in BASIC! In fact, I had the same problem a few weeks ago and built the interface board already. If you drop over to my house this evening, I'll show you how it works and give you an EROM." The look on Jerry's face was one of relief, but I was sure he'd eventually realize I could have answered his question when he first walked in. It was

important that he understand what he was trying to accomplish as well as obtain satisfactory results.

This seems like an overamplified introduction to a simple construction article, but I find it easier to present such topics if I explain how I got involved with them. There's no reason that read only memory programmers should remain as black magic to the personal computer enthusiast. There are a number of 2708 EROM programmers on the market in the $100 to $150 range. But most of the readers who correspond with me say they only want to program one or two for bootstraps and the like. It is for this reason I'd like to present a $9 EROM loader which, when tied to parallel ports such as those described in a previous article (November 1977 BYTE, page 10), can provide this function. Rather than be completely confusing, maybe I ought to start at the beginning.

What Is an EROM?

If you presently own a personal computer, even in its minimum configuration, it contains programmable memory. Most likely the memory you own is made of semiconductor memory chips configured as boards with 4 K, 8 K, 16 K or more bytes. Programmable memory means that any element can be addressed and read from or written to (that is to say, programmed) individually. Addressing is random and is determined by program necessity rather than configuration. Any number of electronic elements can function as programmable memories. TTL 7474 flip flops, bistable relays, core memory, etc, can all function in this manner, but are not necessarily cost effective for personal computer applications. Since the majority of programmable memory storage in personal computers is of the semiconductor type, one major problem is created. Semiconductor programmable memory is volatile. When the power is removed, the data is destroyed.

One solution to the volatility of semiconductor programmable memory is to configure a certain quantity of the storage as nonvolatile read only memory (ROM). ROMs exhibit the same random addressing capabilities as volatile programmable memory, but the data stored in them is permanent. The required bit patterns are programmed into them during manufacture, or during a special postmanufacturing procedure, and any time power is applied, these bit patterns will be the same. Most computer systems containing read only memory use this vehicle to store bootstrap loaders or monitor routines that allow ease of system startup.

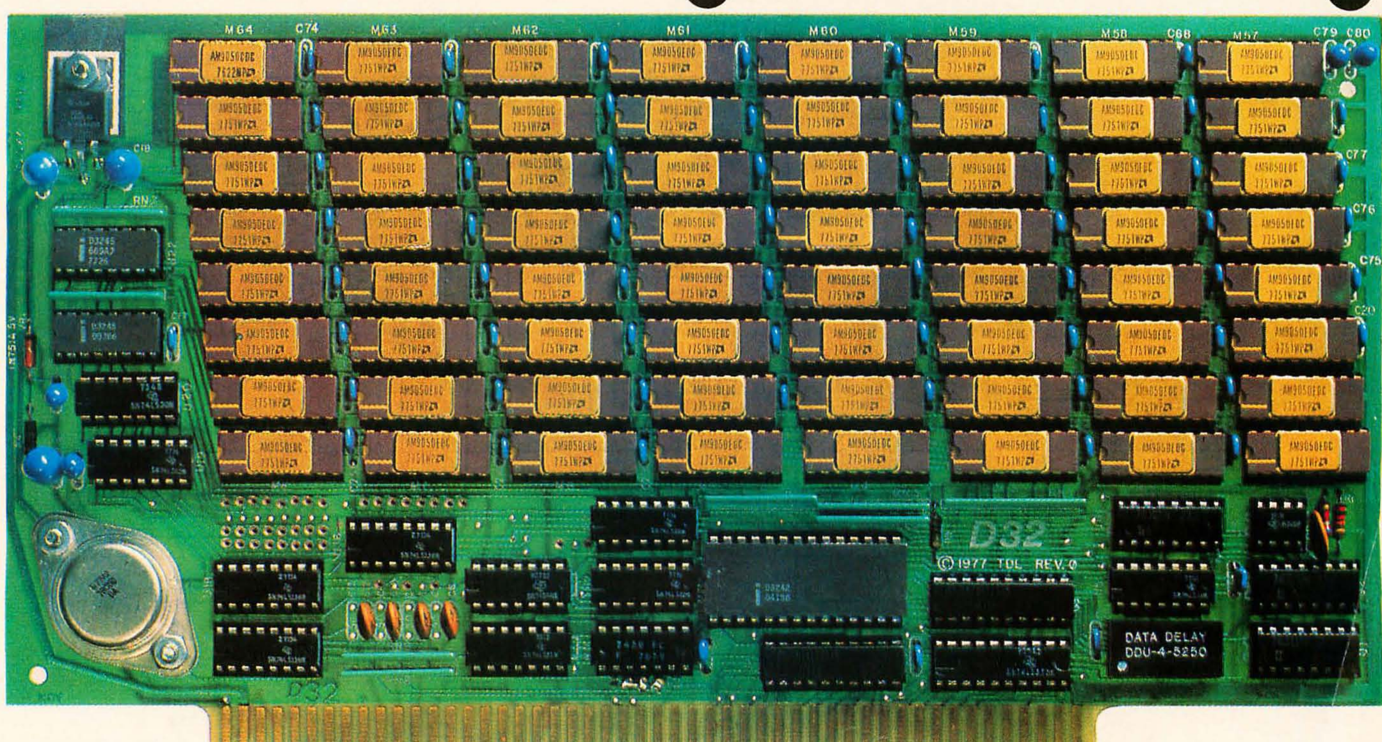
A further extension of the read only memory is the programmable read only memory, or PROM. When a programmable read only memory comes from a manufacturer, no program data is stored in the device. To use this type of read only memory, a special programmer is required to alter the internal structure of the chip and impress specific bit patterns permanently into the addressable memory locations.

It is often desirable to have the nonvolatility of ROMs and the read and write capabilities of semiconductor programmable memories. An effective compromise is the EROM or erasable read only memory. It is used as a read only memory for extended periods of time, erased occasionally and reprogrammed as necessary. Erasure is accomplished by removing the EROM integrated circuit from the system and exposing the chip (covered by a transparent quartz window) to ultraviolet light. I'll describe erasure and programming later.

The erasable read only memory technology used by Intel and most other manufacturers is a stored charge type called a FAMOS transistor, for *floating gate avalanche injection metal oxide semiconductor.* It is similar to what is known as a P-channel silicon gate field effect transistor with the lower, or "floating," gate totally surrounded by an insulator of silicon dioxide. The 1 or 0 storage value of the FAMOS cell is a function of the charge on the floating gate. A charged cell will have the opposite storage output of an uncharged cell. By applying a 25 V charging voltage to selectively addressed cells, particular bit patterns making up the program can be written into the memory. This charge, because it is surrounded by insulating material, can last for years. When this silicon dioxide insulator is exposed to intense ultraviolet light, it becomes somewhat conductive. The result is erasure of all programmed information as the charge leaks away.

There are many erasable read only memories on the market: 1702s, 2708s and 2716s are the major ones. For the most part, experimenters have moved away from the very difficult-to-program 1702s toward the more desirable and more easily programmed 2708s. An added benefit is the fourfold increase in storage capacity of the 2708. The 2716 is the newest version of this erasable technology on the market, and at the time of this writing is considerably more expensive than the 2708. It is for this reason that the methods outlined in this article are used for programming 2708s.

Fastest S-100 Dynamic Memory



5Mhz D-32 Dynamic Memory Board

The D-32 is the fastest S-100 memory board available.

Highest Speed

The D-32's high speed is based upon precise control of timing and conservative design. It operates in S-100 bus systems with cycle timing independent of the bus.

Memory cycle timing is derived from a precision digital delay line, which is four times more accurate than other techniques. Power consumption is minimized by the performance of dynamic refresh cycles only when required and by timing them with a 35khz oscillator. During normal program execution, refresh cycles occur following instruction fetch (MI) cycles, and are fully transparent.

Maximum Reliability

The D-32 is as reliable as static memory boards, since close attention has been paid to the proper engineering discipline to maximize reliability. These details include: the use of molded ceramic bypass capacitors for superior noise immunity, keeping trace lines to the edge connector to a minimum to suppress noise spikes on the bus, precisely-controlled timing and a multi-layer PC board with internal power and ground planes for superior noise immunity.

Expandability

The D-32 has a fully-transparent, dynamic refresh. Each 4096 byte block is addressable at any 4K page boundary. Extended address selection allows expandability to one megabyte co-resident in the system.

MI OP-CODE FETCH — T1 T2 T3 T4 | MEMORY WRITE — T1 T2 T3 | MEMORY READ — T1 T2 T3

Ø2, PSYNC, MI, MWRITE, SMEMR, CE, BUSY, DATA, ADDRESS, REFRESH — TA

REFRESH CYCLES OCCUR TRANSPARENTLY FOLLOWING MI CYCLE READ ONLY WHEN REQUIRED BY INTERNAL REFRESH TIMING CIRCUIT. ACCESS TIME TA = 280 nsec FROM PSYNC (MAX)

MEMORY TIMING IS PRECISELY CONTROLLED USING A TAPPED 250 ns DIGITAL DELAY LINE. TIMING SHOWN IS FOR TDL's ZPU-2 RUNNING AT 4mhz (T-CYCLE = 250ns)
MEMORY WRITE CYCLES ARE INITIATED BY THE LEADING EDGE OF MWRITE PULSE.
MEMORY READ CYCLES BEGIN AT THE LEADING EDGE OF PSYNC (OR PSYNC · Ø1) WHEN SMEMR = 1

Main Features

- immediately available, fully assembled and tested
- static board reliability
- 32K byte memory
- fastest S-100 board available
- independently addressable 4-K blocks
- extended address selection for expansion to one megabyte
- 5 megahertz typical performance, 4 megahertz worst-case
- cycle timing independent of S-100 bus
- precision digital delay line for highest speed
- fully-transparent dynamic refresh
- lowest power consumption
- internal ground plane to increase noise immunity
- S-100 compatible

Immediate Availability

The D-32 is immediately available at more than 125 TDL dealers nationwide. They will show you this fully-assembled, tested and burned in D-32. If your dealer doesn't carry TDL hardware/software products, write or call:

Sales Department • Technical Design Labs Inc.
Building H • 1101 State Road • Princeton, N.J. 08540
609-921-0321
Cable Address: XITAN PRIN • TWX 510-685-9280



Circle 123 on inquiry card.

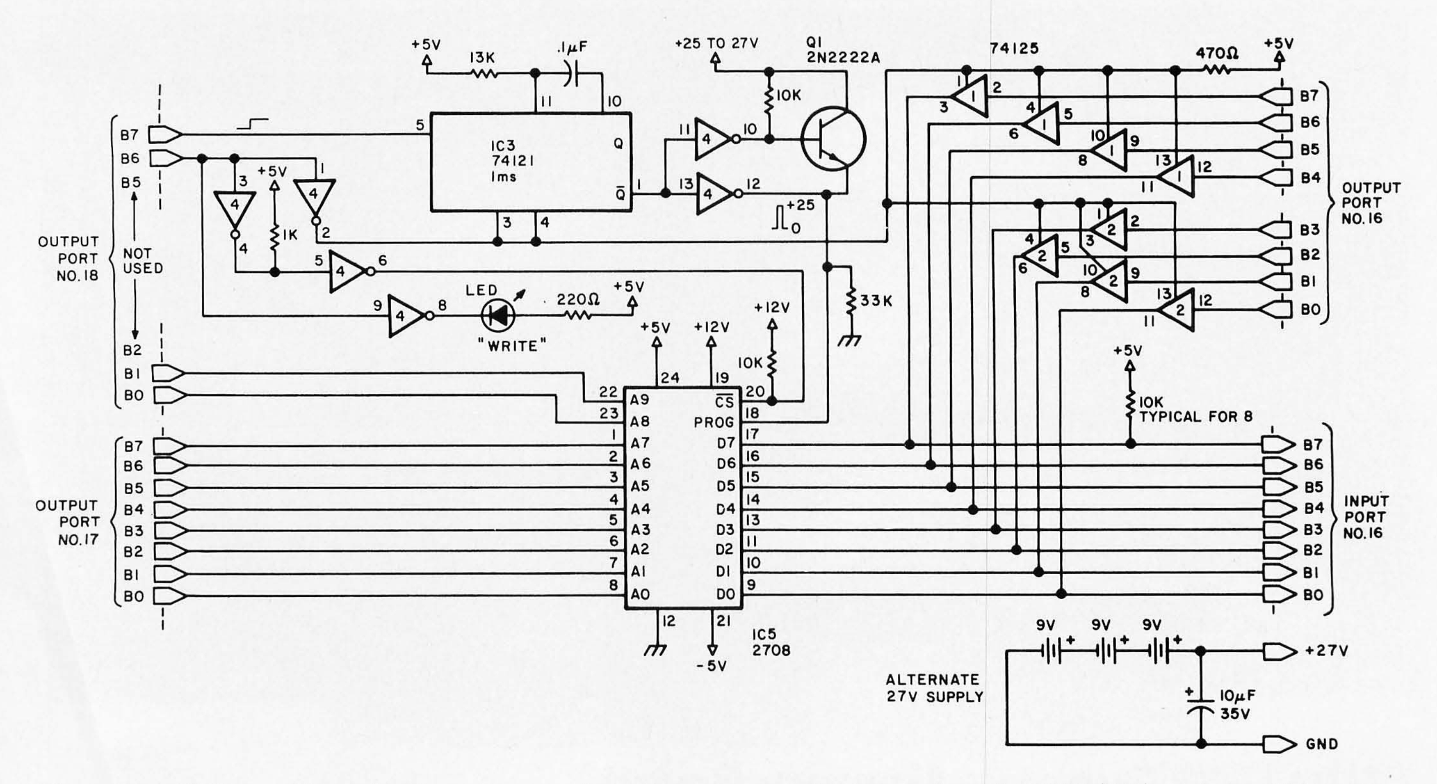


Figure 1: A 2708 erasable read only memory reader and programmer. During reading, the 2708 (IC5) receives a 10 bit address on address lines A0 thru A9. The eight bits of data stored at that location will then appear as outputs on lines D0 thru D7. The circuit is shown attached to three 8 bit output ports and one 8 bit input port of a microcomputer. (The port numbers chosen are peculiar to the author's system and are necessary to fully describe the software interaction.) During programming, bit B6 of output port 18 is set high, which causes the interface to enter the write mode. This signal raises the voltage level on the 2708 select pin 20 from a 0 V read enable to a +12 V program mode enable. The eight data output lines now become data input lines. The program mode signal also gates output port 16 through ICs 1 and 2 to these data input lines and presents the data to be stored to the 2708. Each 8 bit data byte is then burned in for 100 ms in 1 ms pulses using ICs 3 and 4.

IC	Type	+5 V Pin	−5 V Pin	+12 V Pin	Gnd Pin
1	74125	14			7
2	74125	14			7
3	74121	14			7
4	7407	14			7
5	2708	24	21	19	12

Notes:

1. All resistors are 1/4 W 5% unless otherwise noted.
2. Transistor Q1 is rated for VCE = 40 V. Suggested type: 2N2222A.
3. Note that IC4 is a 7407. A 7417 should not be substituted.
4. Programming pulse voltage should be between 25 to 27 VDC.

Output Port 18

B6	B7	
0	X	Read.
1	0	Program mode enabled.
1	_⌐	Low to high transition. Initiates input byte storage into EROM.

("X" indicates a "don't care" condition.)

Programming a 2708

The 2708 is an ultraviolet erasable read only memory. It is configured as 1024 single byte memory locations (eight bits per byte). Figure 1 illustrates a simple interface that allows the user to both read and program a 2708.

When reading the contents of the memory, a 10 bit address is presented to address lines A0 thru A9, and the eight bits of data stored in that location will appear as outputs of the memory on D0 thru D7. The interface is attached to three 8 bit output ports and one 8 bit input port. 10 bit addressing is accomplished by using two bits of port 18 in addition to the eight bits of port 17. When B7 and B6 of port 18 are at a zero level, the 8 bit stored data is read by input port 16. The port numbers chosen are peculiar to my system. Any four user defined available parallel IO ports that accomplish the same functions can be chosen instead, substituting for the ports I used.

Programming is straightforward. B6 of the output port 18 is raised to a 1 level to

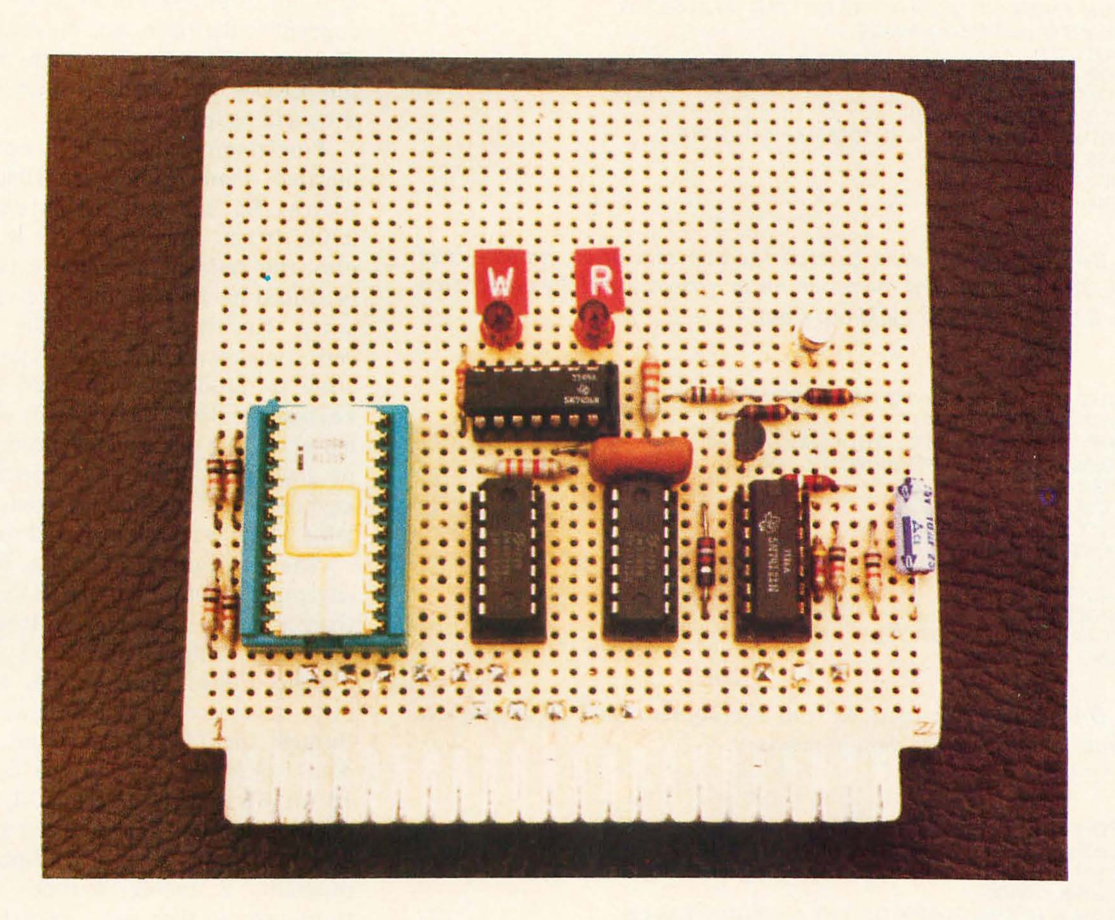


Photo 2: A 2708 programmer built from the circuit in figure 1. This board uses parallel IO ports to set data and address.

set the interface to the write mode. This signal raises the voltage level on the 2708 chip select pin 20 from a zero volt read enable to +12 V program mode enable. The eight data output lines now become eight data input lines to the memory. The program mode signal also gates output port 16 through a pair of 74125s to these data input lines and presents the "data to be stored" to the 2708.

According to the manufacturer's specifications for the 2708, it takes 100 seconds to fully program or "burn in" the EROM. A little simple division would lead one to believe that each address byte should be programmed for 100 ms. Yes and no! Each byte has a cumulative programming time of 100 ms, but it is done in 1 ms pulses. All addresses must be cycled through the program sequence before repeating the pulse on a particular location. In plain English, as each byte is addressed it is given a 1 ms program pulse. To accumulate 100 ms per byte, the program must be repeated 100 times. More on this later.

IC3 and two sections of IC4 provide the +25 V program pulse to the 2708. IC3 is set for a duration of 1 ms and is triggered by a logic 0 to 1 transition at its input. The 2708 both sources and sinks current through programming pin 18, so a combination of devices is necessary rather than a simple open collector driver. In the write mode, when $\overline{CS}$/WE pin 20 is at +12 V and between programming pulses, pin 18 has to be pulled down by an active device because it sources a small amount of current. The 1 ms programming pulse itself is about 30 mA and cannot be easily accommodated without emitter follower configured Q1. This pulse should be between 25 and 27 V at pin 18. Three 9 V transistor radio batteries will suffice for this application or a commercial 24 V, 50 mA power supply can be used. Most supplies can be resistor trimmed to produce the desired 25 to 27 V.

Using the Interface with BASIC

The logic behind this interface is simple: set an address and read data, or set an address and write data. Every EROM programmer I have seen uses an assembly language routine to sequence the operation. This interface is no exception. It will run faster if controlled in that manner, especially if wired to the memory bus for read operations rather than through IO ports. It does not have to be controlled through BASIC.

BASIC is the predominent high level language in personal computer use today.

```
100 REM FIRST WE CLEAR THE OUTPUT AND SET IT
110 REM TO THE READ MODE
130 OUT 18,0
140 FOR N=0 TO 3
150 FOR M=0 TO 255
155 OUT 17,M : OUT 18,N
160 PRINT "ADDRESS "; (N*256)+M;"=";INP16
170 NEXT M
180 NEXT N
200 END
```

Listing 1: A BASIC program used to read the contents of an erasable read only memory. This program and the programs in listings 2 and 3 were written in 8 K Zapple BASIC marketed by Micro Com.

```
100 OUT 18,0 :REM SET TO READ MODE
110 LET X=26000 :REM
114 REM SET X=DECIMAL ADDRESS OF THE
115 REM START OF THE MEMORY TABLE
120 FOR N=0 TO 3
130 FOR M=0 TO 255
135 OUT 17,M:OUT 18,N
140 POKE X, INP16
150 LET X=X+1
160 NEXT M
170 NEXT N
180 PRINT "TABLE LOADED"
200 END
```

Listing 2: A BASIC program used to read the contents of a 2708 erasable read only memory and store the data in memory.

```
90  FOR T=1 TO 100
100 LET A=64 :OUT 18,A :REM 64 IS BIT 6 SET
110 REM THIS SETS THE INTERFACE TO THE PROGRAM MODE
120 LET X=26000
130 REM X IS THE START OF THE MEMORY TABLE
140 FOR N=0 TO 3
150 FOR M=0 TO 255
155 LET D=PEEK X
160 OUT 17,M : OUT 18,N+A :OUT 16,D
165 REM LINE 160 SETS THE ADDRESS + DATA BYTES
170 OUT 18,N+A+128 :REM 128 IS THE PROGRAM PULSE BIT
180 OUT 18,N+A :REM RESET B7
190 LET X=X+1
200 NEXT M
210 NEXT N
220 LET M=0 :LET N=0
230 NEXT T
240 PRINT "DONE"
250 END
```

Listing 3: A BASIC program used to program a 2708.

It is only natural for an experimenter proficient in BASIC to consider using this method. It is important to remember that most BASIC systems use interpreters and will perform operations very slowly compared with assembly (machine) language programs; but, if fast operation is not a particular requirement, BASIC can perform the same functions.

Reading the contents of a 2708 is a simple procedure, as shown in listing 1. Obviously, it takes a long time to print the 1024 bytes in the memory chip even though formatting would speed it up. Another operation which is useful is to read the 2708 and load it into memory, such as in the case of a utility program or interface driver. The concept is the same, but the print statement is deleted. The new program, which reads the EROM and loads it into memory, is shown in listing 2.

Programming the 2708 is no more complicated than reading it. There are two sources for the data to be placed in the 2708. It can come from a 1 K byte listing presently resident in memory (such as that produced by an assembler), or via keyboard entry. Keyboard entry, while possible, is very time-consuming and requires that an array be produced with 1024 variables. If keyboard entry is desirable, it would be far better to use an existing resident monitor program to load memory directly from the keyboard and produce a memory-resident table which is then transferred to the 2708.

The program write pulse timing takes advantage of the fact that BASIC is slower than assembly language. To load a memory with data, output port 18 bit B6 is set to a logic 1 level. This enables the program pulse generator, IC3, and data input source through the 74125s. After the address and data words are sent to the outputs, port 18 bit B7 is raised to a logic 1, causing the oneshot to fire. The duration of the pulse is 1 ms. If this were an assembly language program, a timing routine would have to be used to time out 1 ms before stepping into the next address and data combination. BASIC takes approximately 5 ms to interpret and execute each of the commands used in this program. With such interpretation delays, the program can't possibly overdrive the programming sequence, and therefore needs no timing loops. As stated earlier, to meet manufacturers' specifications, 100 1 ms sequences must be performed. *[If you reprogram the algorithm for another language, or use a BASIC interpreter, make sure the timing is comparable. . .CH]* Such a program is shown in listing 3.

How About a 2 Minute 2708 Write Cycle?

This program is not very fast, and in fact, takes 30 to 40 minutes to run for the full 100 loops. This is fine if you aren't in a hurry, but a better way is to write an intelligent programming routine. Yes, the manufacturer states that to be absolutely sure the 2708 is programmed, 100 loops should be executed. But, it has been my experience with the many 2708s I've programmed using this interface, that it takes only one loop. This is not to say that all devices will perform similarily, but it does lead to some interesting programming compromises. Eliminate the FOR and NEXT loop at lines 90 and 230 in listing 3. Next, at line 230, insert

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Photo 3: An Ultra Violet Products UVS-IIE ultraviolet eraser for 2708s and similar erasable read only memories. This unit can hold four circuits at a time on conductive foam inside the tray.

a program that will read the data. After each complete loop, read the 2708 byte by byte and compare it to the source table in memory. If it is equal, then stop. Programming is done. If any one or more bytes do not correspond, return and sequence through another complete program cycle. In my experience with premium 2708s, I have yet to require a second loop. This will allow fast temporary writing for program checkout. When the software is finalized, reprogram the 2708, when time allows, with the full 100 loops to ensure longevity of the stored data. While conceptually it may seem more feasible to rewrite only errant data bytes, in practice this is not advised.

Erasing an EROM

When 2708s are bought directly from a manufacturer they come completely erased (every byte is hexadecimal FF). If you plan to write a 2708 program once and you either don't want to modify it or you don't make mistakes, forget about erasing. The majority of experimenters will undoubtedly want to reprogram 2708s and similar erasable read only memories. It then becomes necessary to know how to erase them. We all know that the 2708 is ultraviolet erasable. However, duration, distance from the light source, and intensity determine the quality of the erasure.

People concerned about maintaining manufacturer's specifications during the programming sequence should also be advised of the proper erasing methods. Unlike the test-read-after-write loop method for programming, 2708s are usually removed from the circuit during erasing. It is therefore advisable to perform the procedure correctly or it will have to be repeated.

The typical 2708 can be erased by exposure to high intensity shortwave ultraviolet light with a wavelength of 2537 Å. The recommended integrated dose (ultraviolet intensity X exposure time) is 12.5 Watt-seconds per square centimeter (Ws/cm^2). The time required to produce this exposure is a function of the ultraviolet light intensity.

Choice of a particular ultraviolet eraser should be equally divided between cost and safety. A commercial unit not only specifies its intensity (which allows computation of exposure time), but also includes some very important interlocks. It is conceivable that some homebrew erasers might have improper shielding that can allow the ultraviolet light to escape or be accidently turned on while being viewed. Such possibilities can lead to permanent eye damage.

One of the most cost effective erasers on the market is the UVS-11E by Ultra Violet products in San Gabriel CA. This $59.50 unit is made especially with the home computer market in mind and includes some very important safety features. The lamp will not operate unless properly seated in its holding tray and, if lifted from the tray, will automatically shut off. At the standard exposure distance of 1 inch (2.54 cm), the UVS-11E produces an intensity of 5000 μW per square centimeter ($\mu W/cm^2$). Exposure time for the 2708 is easily calculated. Exposure time (T_E):

$$T_E = J/I$$

where:

J = required erasure density of device,
I = incident power density of eraser.

For a 2708 which requires 12.5 Ws/cm^2:

$$I = 5000\ \mu W/cm^2,$$
$$J = 12.5\ Ws/cm^2,$$
$$T_E = \frac{12.5}{5000 \times 10^{-6}} = 2500 \text{ seconds;}$$

or

T_E = 41.6 minutes for complete erasure.

Circle 115 on inquiry card.

In Conclusion

"Well, Jerry, it wasn't all that bad, was it? We got your 2708 programmed with plenty of time to spare and now you know how easy it is to do it yourself." I sensed he felt relieved that he didn't have to cancel his grand computer expo for the computer club that evening.

"Thanks, Steve. I knew that anyone with as much computer junk in his cellar as you have had to have the solution to my problems. It's so much easier when you're working with someone experienced in these matters."

The temporary glow produced by his first statement quickly subsided. I got this strangely familiar tinge of pain as I started to recognize the now familiar line. Other coworkers had involved me in computer gambling and stock market schemes that turned into real fiascos. Rather than argue in my defense, I just shrugged off the desire to take the 2708 back from Jerry, throw it on the floor, and jump on it. How do I get myself into these things? Sanity prevailed and I just said softly, "We'll see."

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Continued from page 83

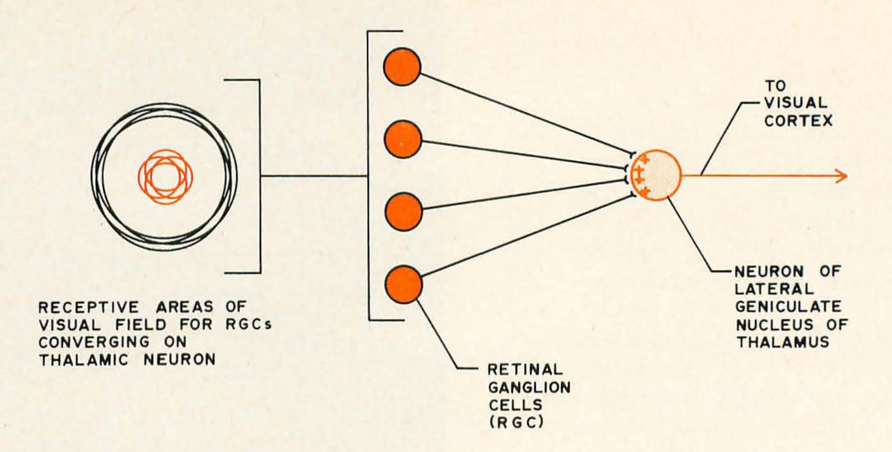


Figure 6: The convergence pattern of retinal ganglion cell (RGC) units on a thalamic cell, showing the spatial relations of the receptive fields of the RGCs which project to the same thalamic cell.

they have response patterns rather similar to the RGCs. That is, central spots and oppositely acting surrounding rings, etc. The active fields tend to be somewhat larger, but it appears that the thalamic cells receive positive inputs from RGCs whose positive centers are close together, so that essentially the same pattern is maintained. This is illustrated for a typical "on-center, off-surround" thalamic cell in figure 6. Actually, at this level there is a great deal of additional processing going on that has to do with modifications on the basis of data returning from the cortical areas to which the thalamic cells project, and also data from other brain regions which have input to the visual analysis system. We shall speak more of these other inputs later, but for now we shall follow our line detector system on to the cortex.

The axons of the thalamic cells make contact with a class of cortical cells known as "simple field cells." These cells typically respond preferentially to more complex stimuli, such as lines of light at particular inclinations, and particular locations. Usually, it is found that a column of cortical simple field cells deals with the analysis of some small area of the retinal image, and contains a large number of such line analyzers. Each is responsive to a line at a slightly different angle, but all are concerned with the same small area. Figure 7 shows how such a line detector can be constructed from the output of the thalamic cells. What is required is that the thalamic cells which have a positive influence on the firing of the cortical simple field cell are selected to be ones that have their own circular excitatory centers in the visual field in a straight line at some angle to the vertical. If the inputs to our cortical cell are so selected (selective convergence), then the optimal stimulus for firing it will be a line of light which passes through the excitatory central spots of all the lower echelon thalamic cells' receptive fields. Such a stimulus will produce a strong (but sub-maximal) firing in each of

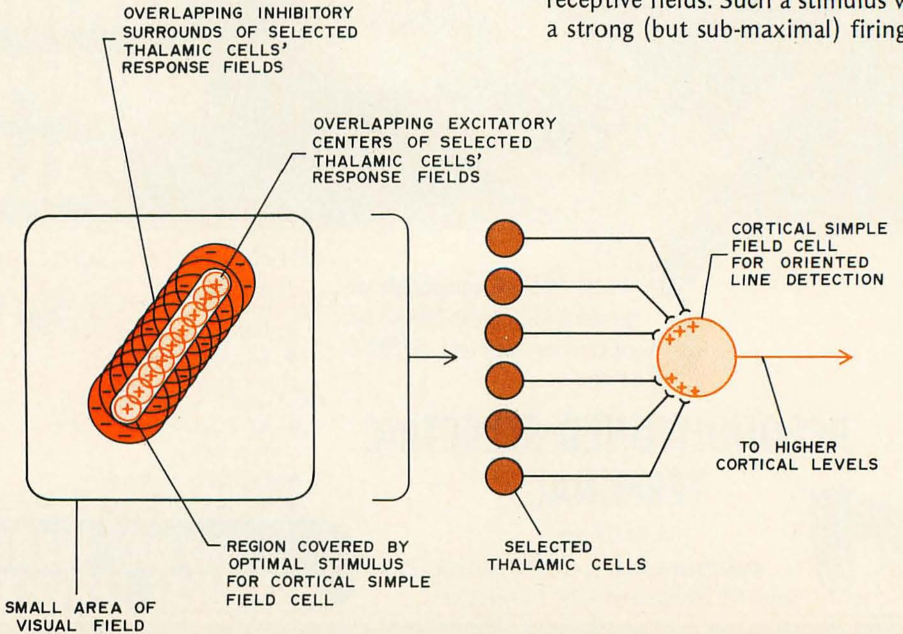


Figure 7: The pattern of convergence of thalamic cells onto a cortical oriented line detector (simple field cell). The spatial relations of the receptive fields of the thalamic cells which project to this cell in an excitatory manner is so chosen that their own excitatory regions lie in a straight line.

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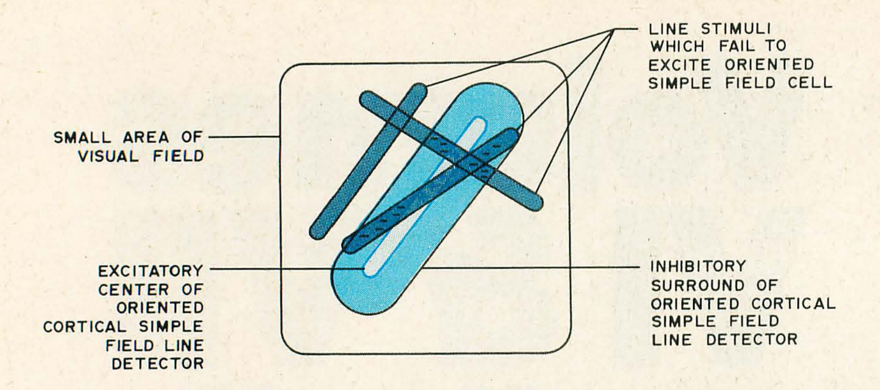


Figure 8: Lines of light which are not optimally placed do not activate the simple field cell since they either do not strike sensitive elements, or strike excitatory and inhibitory areas equally.

the thalamic cells since it will intersect some of the inhibitory territory of each, but such a sub-maximal output from *each* of them is the maximal input for the cortical level cell. Now look what happens if the line is turned at a different angle, or moved to a different position as in figure 8. If the angle is not aligned with the line of the "on-centers," one thalamic cell will show a positive response; but the others will not, and may have their inhibitory areas activated. There is thus little input to the cortical line detector. If the line is kept at the correct angle, but moved to the side, it falls in all inhibitory territory, or else beyond the active region altogether. Thus, while our simple field cell can discriminate angle, it also discriminates location.

The next level of abstraction is reached with the so-called "complex field cells" of the cortex. A typical example of one of these would be a cell of the type we have been seeking, one which would respond to a line at a specified angle, located anywhere in a large area of the visual field. Such a cell is easily constructed if it can OR gate the outputs of a large number of simple field cells, all of which respond to a line at the same angle, but whose specific sensitive locations with regard to retinal position differ, and are spread over a wide area, as shown in figure 9. Again, certain convergence patterns are selectively implemented. In this case the convergence principle is parallelism.

In actuality, the connections are not so straightforward as I have suggested; there is much up and down traffic from thalamus to cortex and back. There is much up and down traffic between different levels of the cortex as well. The principle however is essentially as illustrated. By continuing this type of operation, and by combining outputs of different types of cells, it is clear that feature extractors of any desired degree of complexity could be built. Arc detectors, edge detectors and numerous other types are already available at the simple field cell level. At the level of more complex feature extractors, which may be in areas of cortex outside the primary visual cortex, it is very difficult to determine the effective stimulus for a cell simply because of the enormous number of stimuli that it might respond to. In a monkey brain, for example, a cell has been reported by one researcher which responded only to the outline of a hand. It is not necessary for us to specify all these types of feature extractors for our purposes. The particular set that was most useful to a human's brain would probably differ from the most useful set for a robot brain. It is sufficient to see the principles by which the feature extractors can be constructed. Let us review these.

First, it is clear that not all possible combinations of retinal receptor activa-

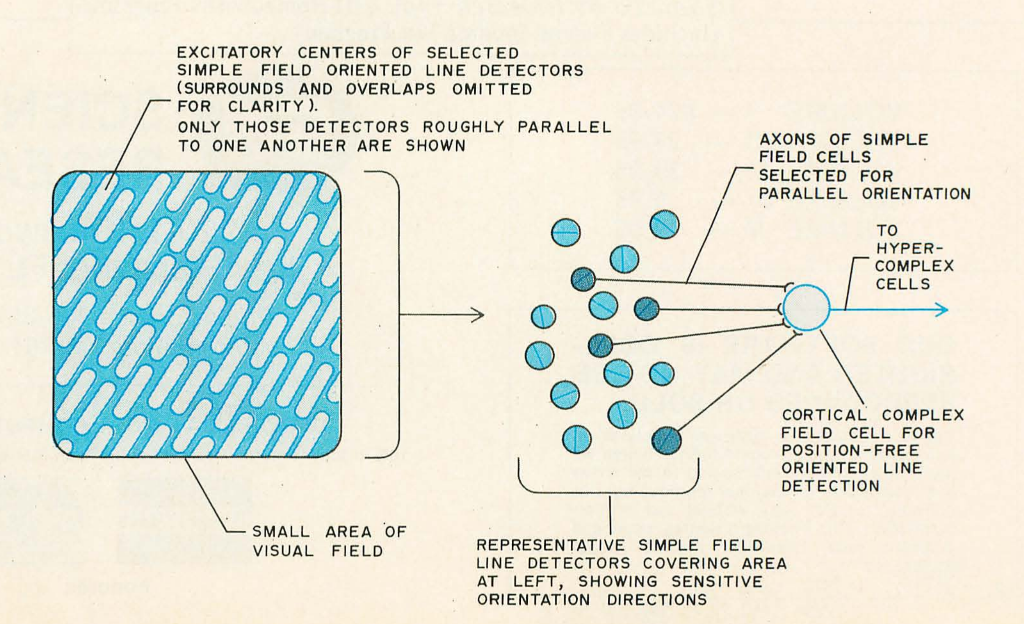


Figure 9: The development of a complex field cell of the cortex which responds to lines at certain angles, but without reference to spatial location over a large retinal region.

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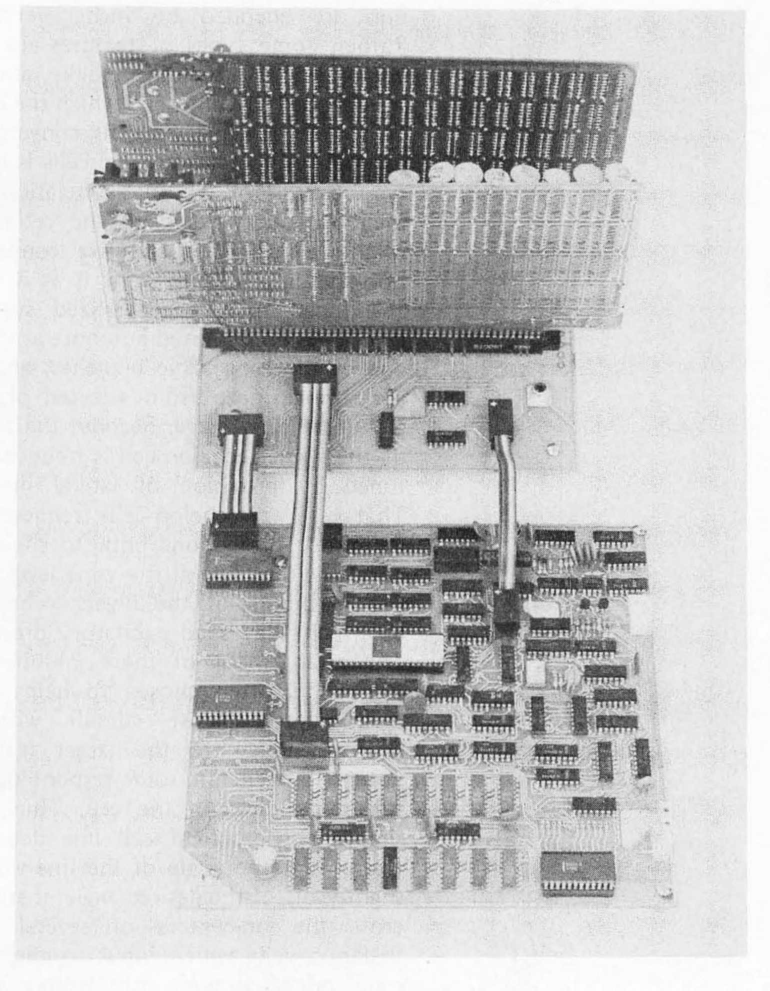
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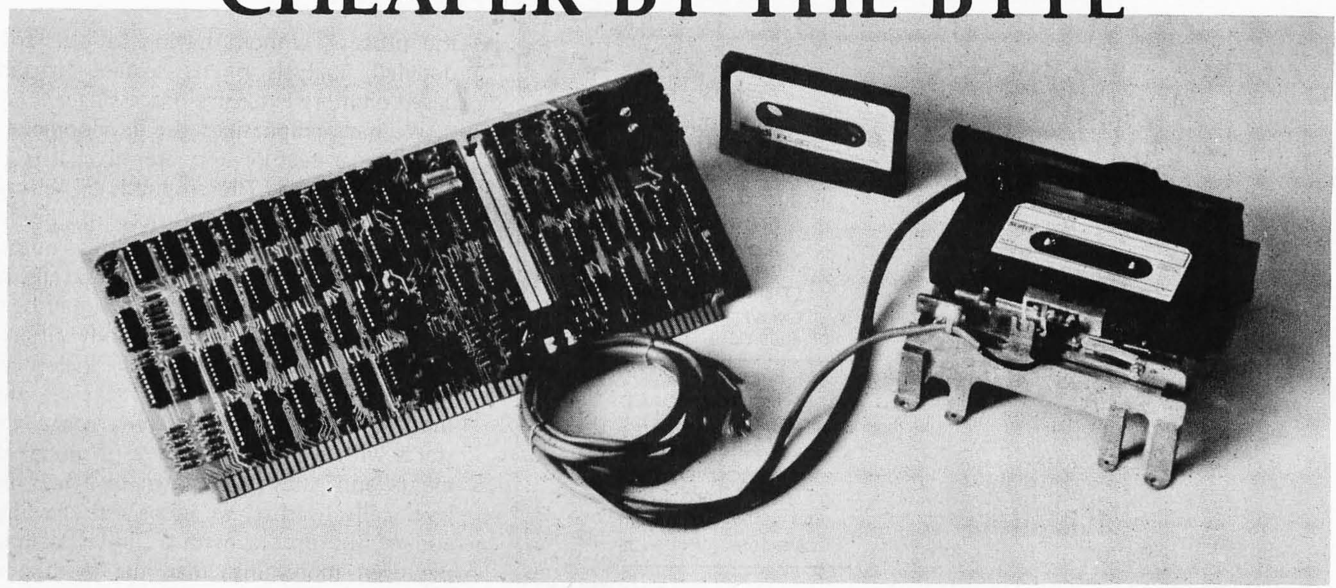
tion are encoded by higher level cells. Rather, some types of features are settled upon as useful building blocks, and these are encoded by cells upon which the outputs of certain lower level cells converge. The particular set of lower level cells is selected on the basis of the spatial relationship of their receptive fields on the retina. This is the principle of selective convergence. Look again at figure 2; it is as if we had abandoned such a generalized system in favor of a more limited but more economical one by omitting some branches, and bringing several more from selected places together at each stage. Second, the response of the higher echelon cell is frequently fine tuned by provision of lateral inhibition. That is, lower echelon cells frequently have inhibitory projections both to their neighbors to either side at the same level, and to the neighbors of the higher echelon cell to which they send excitatory projections. The arrangement of these inhibitory projections is often chosen to help the cell discriminate against stimuli which are similar enough to the target feature to potentially generate some responding, if not full responding, in the cell. Thus, in the simple cortical field cell line detector in figure 8, if the angle of the line were only slightly off of the desired angle, it still might cross the on-centers of several of the thalamic cells which input to the cortical cell, and cause some considerable response in the cortical cell. It should of course only activate some other angle detector. This difficulty is surmounted by the fact that in order to cross the first cell's line of on-centers at a small angle, the stimulus would also have to cross a large amount of territory which inhibited the thalamic cells' output. (If the angular discrepancy is large of course there is little problem.)

The third principle of general relevance is related to the problem of how much input will be required to fire a higher echelon cell. Recall that the neurons are not functioning strictly as AND or OR gates, in that a certain percentage of inputs active is all that is required for firing. This ALMOST gate principle is one of enormous power, and we shall have more to say about its application to intelligence in a later article; but for the moment look at what happens in the sensory system if we let the percentage of inputs required for firing be an adjustable parameter. If we required that all the lines be active as in a conventional AND gate, we would have a perfectly accurate system, like any good conventional computer. We would also have a slow and insensitive system. To get all the inputs properly set up, we would need to wait for perfect alignment of the image, probably close up for good resolution, and have good illumination to avoid any marginal situations. It would be accurate, but your ancestors would never have reached reproductive age if they'd had to wait on that kind of situation before decoding the stimulus as a wolf. On the other hand, if we let the system be sloppy and fire feature extractors when only a small number of relevant input lines are active, we will get quick results, with a lot of errors. In particular, we would be unable to make fine discriminations amongst similar stimuli which would activate many lines in common.

This kind of error is easily demonstrated. Briefly flash a picture of a circle with a small piece missing on a screen, and your subjects will report that they saw a complete circle. Only if they get to examine the image longer will they be able to discriminate the broken circle from a complete one. Now clearly both modes of processing have their uses, and it would be nice to adjust the percentage input requirements of the ALMOST gates to suit the task at hand. This is done in the brain by axons from control regions of the brain outside the sensory system which make diffuse and widespread contact with large numbers of sensory processing elements. These inputs carry no specific visual information, but by excitatory or inhibitory action they can bias the processing elements towards or away from firing threshold, thus increasing or decreasing the amount of input from lines carrying specific information which is required before firing occurs. When this process is driven beyond normal limits, as with various drugs, the feature extractors can be biased so close to firing that little or even no input is required. The result is a variety of visual distortions and hallucinations.

A fourth point worth noting is that the system resembles a pipelining type of processor. As soon as the cells of any echelon have fired in response to the current state of their inputs, succeeding echelons begin dealing with that fact while the earlier echelon begins to respond to the next state of their inputs. It is not clocked, it just all trickles through as fast as it can, but that only means that some things take longer to recognize than others. There is no need for it all to be processed in lockstepped stages like a real pipelining system. However, information can be siphoned off the line at any stage as well as being passed on to the next. If you need to catch a fast moving object, you can respond to information about its position, which is encoded fairly early in

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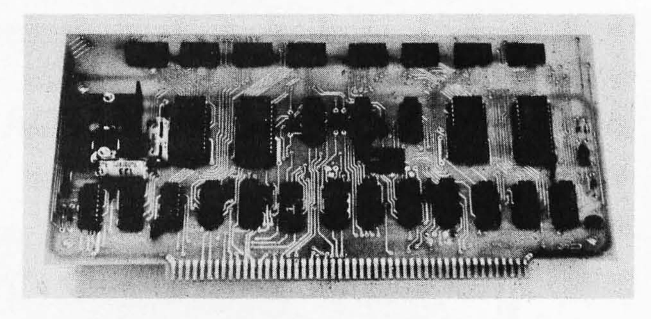
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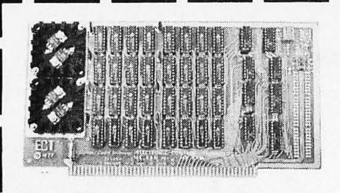
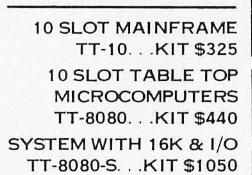
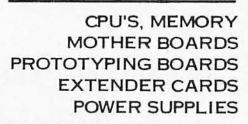
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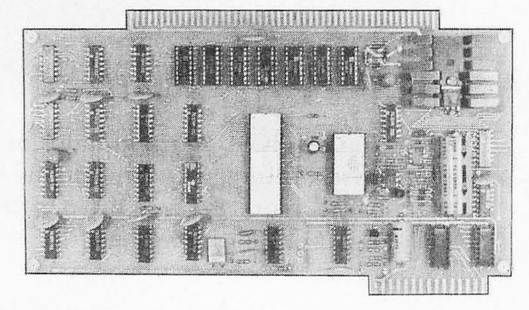
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the process, without having to wait for a detailed analysis of its surface markings based on more extensive processing.

We have emphasized the development of a particular feature extractor to clarify the process involved. The emphasis on selective convergence should not obscure the fact that each lower echelon cell's outputs usually go to many higher echelon cells, not just one. Further, these outputs may be involved in the extraction of entirely different features at each of the higher echelon cells to which they project. It is not the case then that we have a grand convergence that starts with a million bit byte of retinal elements and gates itself down to a few high level cells. Rather, we come out the other end of the process with a "byte" containing even more lines than the input byte. The difference is that the bits in the input byte represent the spatial pattern of illumination on the retina in a simple point for point code. The bits in the output byte of the system each represent the occurrence or non-occurrence of a complex pattern of features in the visual world, and can be used to directly activate appropriate responses. Thus, the input byte and the output byte of the visual system each contain the same basic information — the content of the visual world. However in the output byte the information is recoded so that the bits each represent highly useful pieces of information about the patterns occurring among the input bits. Referring again to figure 2, the real situation would be one in which there were as many cells at the top of the figure as at the bottom, with each convergent tree leading to a top level cell containing many elements in common with other convergent trees, just as the two shown do.

We have dealt so far only with the processing of spatial patterns of retinal illumination. There are many other things which are dealt with; motion detection by sequential activation of retinal elements is one example. Depth perception by comparison of the patterns from the two retina is another. One that deserves special mention here is the handling of intensity information. This is done in the brain by use of the analog information in the cell's "temporal byte." That is, each line carries one bit in the "spatial byte" which encodes the existence of some set of conditions at the retina related to which cells are activated. The rate of firing of the line encodes, in pulse frequency analog form, information about the strength of that activation. For low echelon cells, this is essentially information about the intensity of the light falling on the receptors. At higher echelons in the

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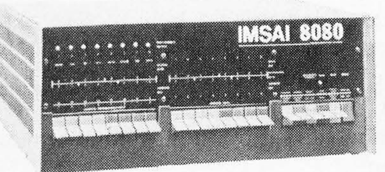
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sensory system, it is information about the "degree of certainty" of the cell in question with regard to its identification of a feature. This information derives from both intensity and spatial information, since both higher pulse rates and more lines active will increase the firing of the cell. This is an example of the way in which the brain may combine digital and analog information in a single decision process. The nature of what is being encoded by intensity at the higher levels of the process may be better understood by applying the "degree of certainty" concept to the lowest levels, where the temporal byte represents light intensity. Obviously the low level element has the greatest degree of certainty that it is being illuminated when it is being illuminated most strongly. At higher levels, number of inputs and activity of inputs can trade off with regard to drive on the receiving cell, and this is generally appropriate, because the degree of certainty about the existence of the feature to be decoded is increased if there is either a broad agreement among the inputs, or if the inputs are themselves "very certain." In general in the brain, "He who yells the loudest has the most to say." Since cells don't have egos, it works.

In any realistic approach with present day hardware, this would probably have to be modeled using a byte of several bits in place of each single line in the brain. "Which byte" would be equivalent to "which axon," and the bit pattern would carry the information carried by the temporal *byte on the* axon.

Given that the number of conceptual features into which the visual world could be subdivided is virtually unlimited, whereas the number of available bits in the systems' output byte is merely enormous, how does the brain decide which features to encode? Some of it, the simplest parts, are undoubtedly the result of evolutionary selection, hardwired at birth. Much of it however is probably developed in response to the type of visual environment in which the animal grows up. There is evidence, for example, that if a kitten is exposed to a visual world containing only vertical lines at a certain period of its development, its visual cortex will be rich in line detectors with a near vertical orientation, and poor in detectors for other orientations. Apparently this pattern persists throughout later life. It seems similar to a PROM.

Finally, we should mention some types of nonvisual input to the process that carry very specific correction information. Try this experiment. Look across the room while moving your head from side to side. Notice

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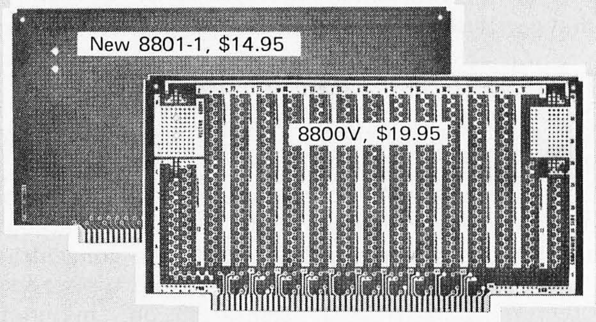
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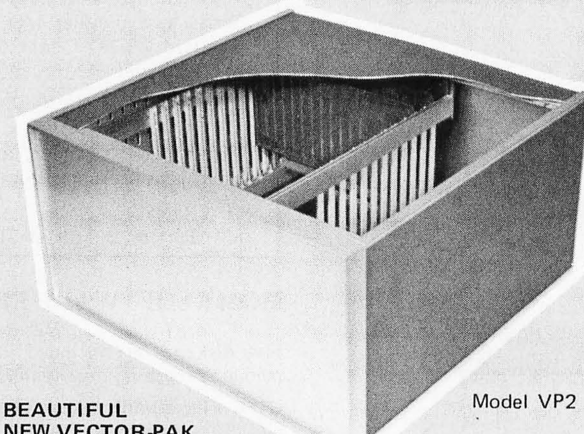
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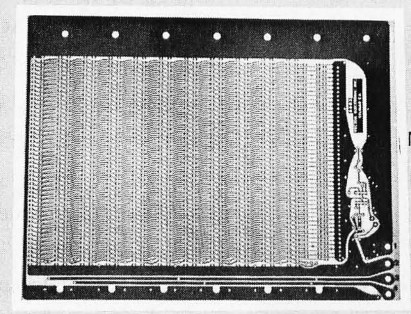
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that the world seems to stay still, even though you are moving its image around on your retina. Now move the image around on the retina in a different way. Place your fingertip against your lower eyelid and lightly jiggle the eyeball while looking across the room (keep the other eye closed). Notice that this time the world seems to jump around as the image is moved about on the retina. Why the difference? In both cases the image is moving around on the retina. The answer is that movement of the image caused by moving the head in the usual manner is naturally an everyday problem for the brain in interpreting the visual world. It solves the problem by using feedforward information from the motor nuclei which control the movement of the head and body to correct the interpretation of the relative motion of image and retina to precisely allow for the motion as it occurs. Since you don't usually go around jiggling your eyeball with your finger (I assume), your brain has never developed a mechanism to precorrect for doing so, and you see the motion. There are more subtle nonvisual inputs to the processing too, such as your motivations, but these are poorly understood and beyond the scope of these articles.

Now the hard part. How might we model such a visual system with current digital technology? As a start, let's examine what would be required of a "brute force" approach if we didn't care what it cost. It would seem the most straightforward method would be to have a set of microprocessors at each echelon modeling the activity of each of the elements at that level. Since with straight digital techniques we would have to code intensity on a byte of several bits length, each lower echelon input element talking to an upper echelon unit would have to present a byte rather than a line. This means (say) eight lines for each converging step and each lateral inhibition, instead of one. Each processor would then accept a number of bytes from elements at a lower level, which it would process according to a small ROM program, and a number of bytes laterally from its neighbors, which data would also figure in the result. The ROM program would determine the type of response of the "cell," and its output would be a byte on a bus that ran to a number of yet higher echelon processors, and laterally to its own neighbors. If we really wanted to model the brain's operation, this would all be conducted with handshaking logic and the processors would all have their own private clocks. Each processor would simply continually compute the result of whatever

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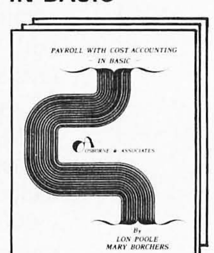
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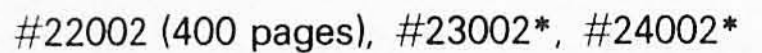
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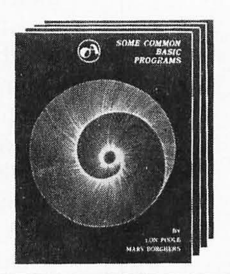


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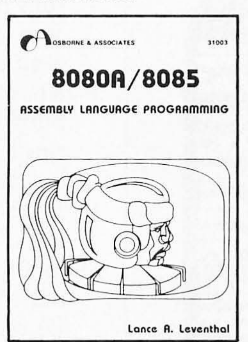




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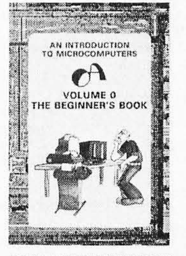
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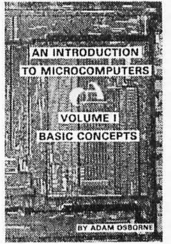
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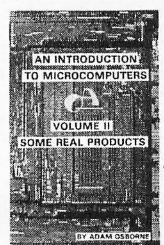
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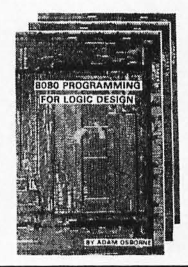
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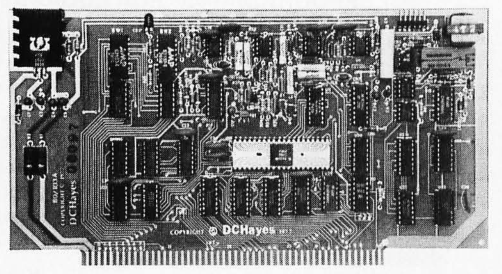
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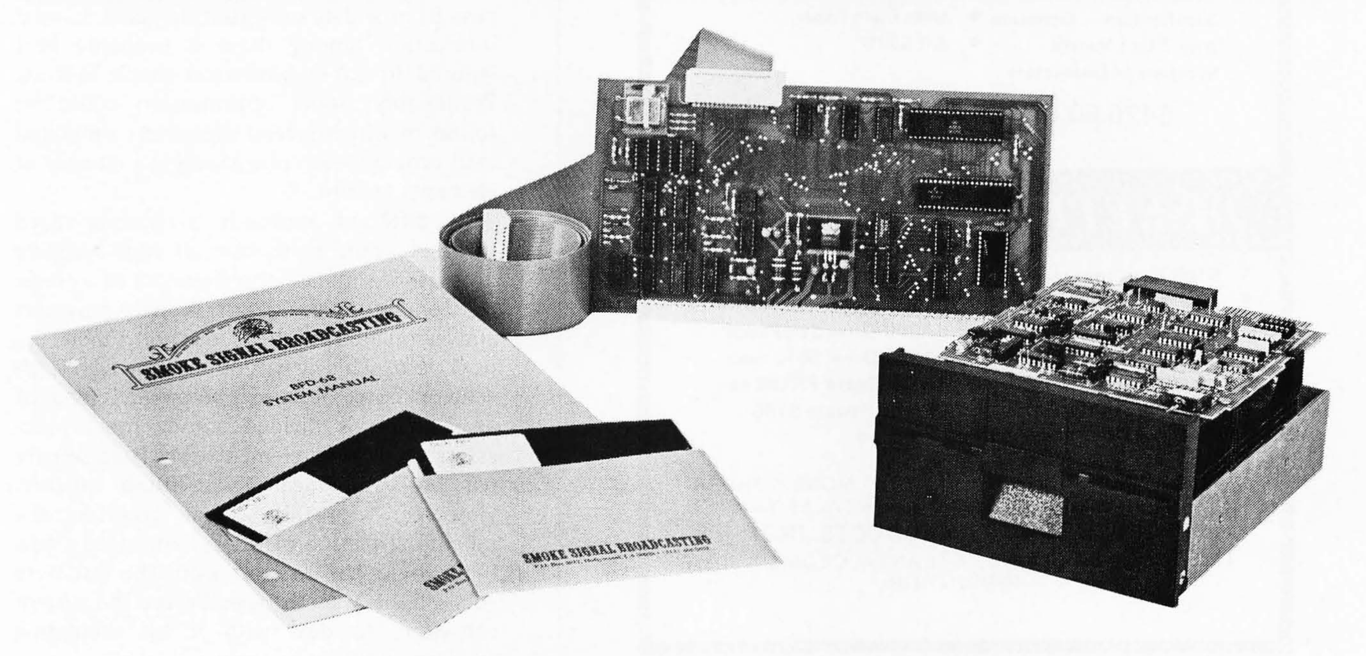
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inputs it had available at any instant and output the result. When the input from any of its information sources changed, the output would change. With a processor and a ROM to represent each cell, such things as the weighting of percentage input from an ALMOST gate action, and the continuous alteration of output on the basis of the output of lateral neighbors, are simple. Such a system would be fast, powerful, and incredibly expensive. Let's say we opted for a minimal system running off a 64 by 64 grid of photosensitive elements. Further let's say we want to keep the ratio of input to output at each echelon approximately unity, so we wind up with about 4,000 highest echelon feature extractors. (Not bad; that means the system can recognize 4,000 different complex stimuli.) Then let's say we want to carry the analysis to a depth of five echelons. (That determines the complexity of the stimuli which can be extracted by the highest level. Remember that the brain only took four echelons to get to the complex field cell. Hypercomplex cells can handle some very advanced extraction problems.) At this point, however, we are talking about 20,000 processors. Even at 8008 prices, that's not exactly cheap.

Now suppose we try to trade speed for cost. The system just described obviously runs much faster than the real brain. A first step might be to have single processors at each echelon doing the work of many, even all, of the 4,000 elements at that echelon. Suppose we could update the output of a single simulated element in 100 μs. That means we could do all 4,000 in each echelon in about half a second. That's not too bad; it's still pipelining the processing from echelon to echelon, so the system would see a picture updated every half second with a (½ second x number of echelons) delay between the stimulus event and the final analysis. Even if we pulled some information off the pipeline early for rapid action, however, it's still too slow for real time work. (If you ever have the equipment at hand, try playing catch in a room illuminated with two per second strobe light flashes. Anything below ten per second gets difficult.) Two complexities also appear when we try to update the simulated elements of an echelon serially. One is that the program for each element is different, which makes our ROM a little more complex. The other is that the output of each element in the array depends in part on the current output of its neighbors, including the ones you haven't gotten to yet in the current pass. With only one pass across the array per update, a "lateral lag time" error would

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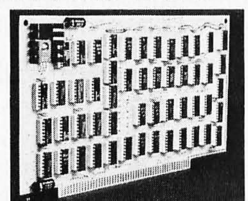
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be introduced. Correcting this with the simple expedient of iterative passes takes too long. Furthermore, you have to carry some information in scratch pad. How far do you want elements to be able to interact laterally? For most purposes, a few elements away might do, but for some tasks such as motion detectors, the brain converges outputs from widely separated elements. Lateral interaction among these is probably best ignored in our hypothetical simple system. Presumably, some optimization could be found in which several processors simulated each echelon, each one handling a number of elements serially.

A different approach to trading speed for cost would be to have all your available processors simulate the elements of a single echelon, store the result, switch programs and simulate the next echelon, then the next, etc. This way you get through each echelon faster because a complete update of an echelon is divided among more processors, and fewer elements simulated serially per processor means you finish quicker. However, with this scheme you lose the pipelining feature of the system, since a new input byte has to wait until the last byte gets all the way through before the system can start to deal with it by simulating echelon number one again.

These notions of course do not exhaust the approaches to the problem, and I didn't promise to solve it for you, but they illustrate some of the kinds of difficulties we can expect to have to overcome. (Actually, I have some more advanced ideas on the subject, but you're not going to hear about those until somebody offers me a vice presidency for Psycho-cybernetic Architecture!) The best approach may well not involve replicating the detailed features of the brain's processing steps in recoding the sensory input. What does seem worth study however is the general logic of the approach. Specifically, this would include such items as: ways of eliminating redundant information, the logic of using selected feature extractors as building blocks at each stage of the perceptual process, the elimination at each level of restrictions such as position on the generality of the feature encoding line, and the use of the ALMOST gate concept to provide continuously variable levels of stringency in the encoding process.■

BIBLIOGRAPHY

Hubel, D, "The Visual Cortex of the Brain," *Scientific American*, November 1963.

Karner, N (trans), *Current Problems in Neurocybernetics,* Wiley, New York, 1975.

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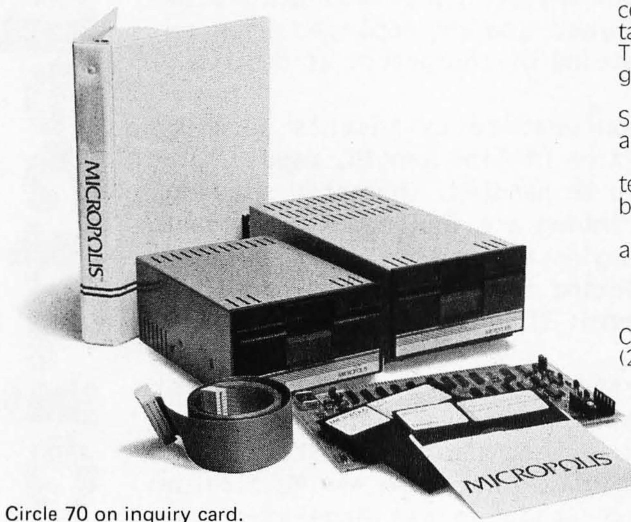
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DS,DV,DP	Diablo Hy-Term	SOL/Cuter,VDM-1/Tarbell,VTI/Tarbell	$150.
DSN,DVN,DPN	Diablo Hy-Term	SOL/NStar,VDM-1/NStar,VTI/NStar	$175.

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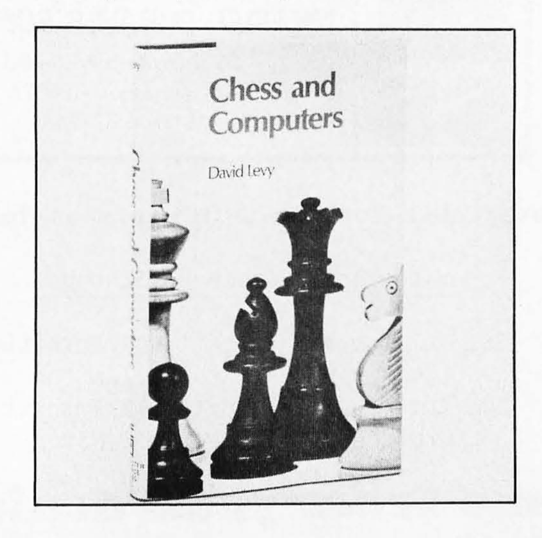
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Book Reviews

Chess and Computers *by David Levy, Computer Sciences Press, Potomac MD, 1976, 145 pages. Paperbound, $8.95.*



If you enjoy playing chess, then you should thoroughly enjoy *Chess and Computers* by David Levy. This 145 page paperbound book is loaded with chess games played by computers. The games are computer versus computer and computer versus human. When you settle down with this book, it would be a good idea to set up your chessboard and play the games. As with any good chess book, half the enjoyment is found in playing along, duplicating the moves in these games, reading the comments by the author, and adding your own comments.

The initial chapter recounts two of the early (1700s) so-called chess playing machines. The automaton chessplayer developed by Baron von Kempelen is detailed with much emphasis placed not only on the sham it produced, but also on the mechanics of the machine itself. The chess playing machine of Torres y Quevedo is also discussed in this initial chapter. Although this machine played a king and rook against a rook endgame, the idea of the tree structure is quite evident in the mechanics of the device.

Chapter 2 is entitled "How Computers

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Play Chess." Needless to say, it requires a second and third reading. Levy assumes the reader has a basic knowledge of chess and chess playing by computer. He introduces the tree structure and its importance to game playing by computer. Some of the chess ideas stressed include: center square occupation; mobility and quantity of pieces; and the subtle features which make the difference between a good and a poor chess player. Any good chess player knows that the secret to winning involves the ability to look ahead throughout the game. In this way, the player is in a position to gauge future game conditions and their values to himself and his opponent. The computer carries this look ahead feature to great lengths. Here is where the tree structure comes into play and Levy includes many details of this important aspect.

Chapters 3 and 4 are historical in that they recount the early and modern eras of computer chess. The early history of computer chess dates to before 1960 while the modern era brings us up to the mid 1970s. Throughout this book, and especially in these two chapters, the games played by computer are listed. This is the time to get out your board and play along with the book. The remarks and the games are well worth reading twice. As you read and play the games listed in these two chapters, you can see that the programs are improved as they grow in age and wisdom.

There are more interesting games in chapter 5. Since this chapter deals with computer chess tournaments, you would expect to see the better games played by computer. You won't be disappointed. The last two chapters concern themselves with future developments in the area of computer chess. Levy also takes time to mention his bet that no computer program will be able to beat him by 1978.

This book offers something for the chess player as well as for the computerist. The games are numerous and the remarks are good. The computer jargon is interesting and nontechnical.

Len Gorney
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The publisher has just informed us that a second volume of Chess and Computers *is due to be published soon.*

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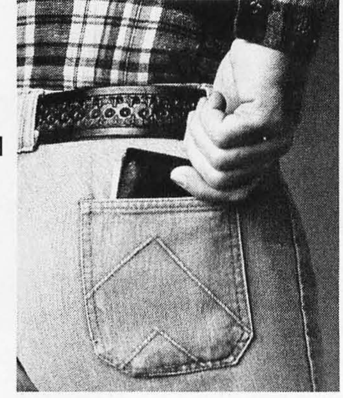
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About the Author

Dan Fylstra is a graduate of Massachusetts Institute of Technology and a second year student in the MBA program of Harvard Business School, concentrating in marketing. His background includes extensive work with high level languages including authorship of the PLM/6800 compiler for Intermetrics Inc, and consulting on the HAL/S language and compilers for NASA and the European Space Agency. His equipment now includes a KIM-1, an OSI system, PET 2001 and Radio Shack TRS-80.

User's Report: The PET 2001

Dan Fylstra
22 Weitz St #3
Boston MA 02134

Photography by Dan Comly

About a year ago Commodore Business Machines Inc, a well-known maker of pocket calculators, startled everyone in the personal computer industry by announcing its PET computer, a self-contained unit with keyboard, display, cassette drive and built-in BASIC for $495. The announcement was greeted with considerable enthusiasm and skepticism, for Commodore obviously was stretching the state of the art in technology, manufacturing and mass distribution.



Photo 1: A view of the Commodore PET, Model 2001. This personal computer sells for $595 and includes a keyboard, video display, cassette drive, 4 K bytes of programmable memory, and a BASIC interpreter and operating system in 14 K bytes of read only memory.

Now the first PETs have been delivered, and a few computer stores have begun advertising their availability. The PET's price has risen to $595, and in the meantime other personal computers with comparable price and performance characteristics have come on the market. Many people are wondering which computer represents the best buy in terms of hardware and software capabilities, expandability, availability and delivery, warranty and service, and software support. If you are considering purchase of such an "appliance" computer, this review should help you make your own informed judgments on these issues.

I ordered a PET a few days after the finished product was shown at the National Computer Conference in Dallas TX last June, and hence I received one of the early units (apparently number 17 off the production line) without a complete user manual describing everything the PET can do. By the time this is printed a better user manual should have been published; so bear in mind that this is a preliminary review, written in late October 1977, and based on experience with my PET, conversations with Commodore engineers at trade shows, and precious little documentation. I have not been able to test some of the PET's many features, in particular the expansion options, due to the dearth of information from Commodore. For a more complete picture, talk to your computer dealer and, if possible, to other PET owners before you make a purchase decision.

General Specifications

Photo 1 illustrates the attractive overall appearance of the Personal Electronic



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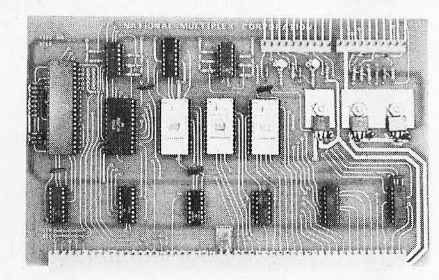
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This is a complete tape controller for the SWTP 6800 system. Has 3 K of EPROM space for your own programs. A 1 K ROM (2708) is provided with all tape and monitor functions. The ROM program is identical to our extensive 8080 ROM program.

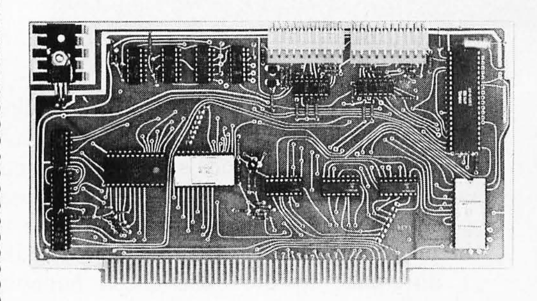
Has one ACIA for one or two tape drives, one USART for an additional Serial port and a 4 bit parallel port for motor control. Will control one or two CC-8 or 3M3A drives with the software provided. Can be used with other tape drives controllable with 4 TTL bits if appropriate software changes are made.

Extra serial port is provided for your use with a second terminal or printer. (RS232, TTL or 20 ma)

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This is Revision 7 of this controller. This version features 2708 type EPROM's so that you can write your own software or relocate it as desired. One 2708 preprogrammed is supplied with the board. A socket is available for the second ROM allowing up to a full 2K of monitor programs.

Fits all S100 bus computers using 8080 or Z80 MPU's. Requires 2 MHz clock from bus. Cannot be used with audio cassettes without an interface. Cassette or cartridge inputs are RS232 level.

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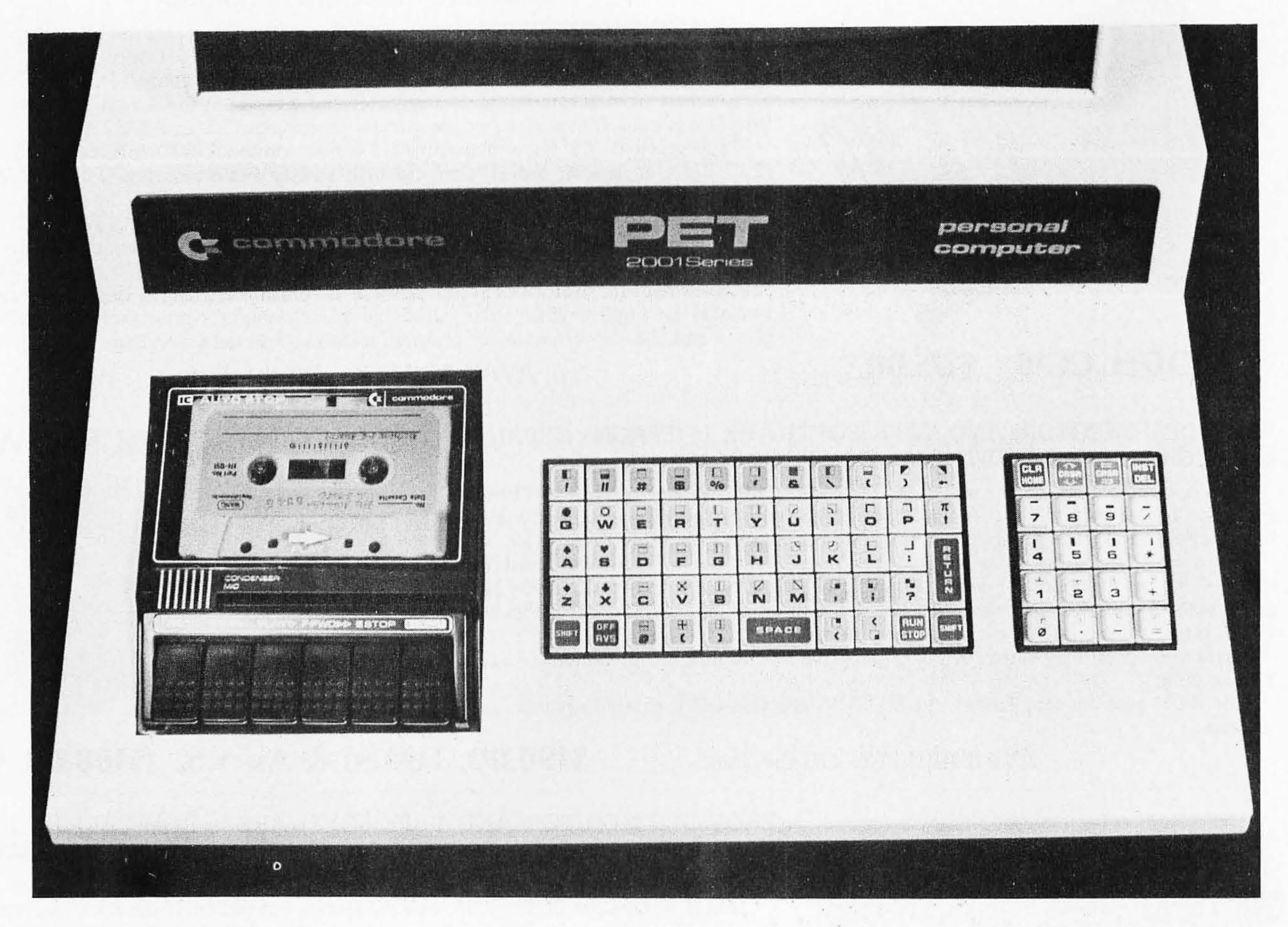


Photo 2: A close-up of the PET keyboard and cassette drive. The keyboard is a flat, calculator style unit with 73 keys. The upper case shift positions on 64 of the keys are occupied by graphic characters. At the right are the cursor control and insert/delete keys and a numeric keypad.

Transactor, Model 2001 (as it is fancifully called). Overall it measures 16.5 inches (41.9 cm) wide, 18.5 inches (47 cm) deep and 14 inches (35.6 cm) high, and weighs 44 pounds (20 kg). The PET is a lot more portable than most computers, but you won't have to carry it very far before you'll appreciate how heavy an oddly shaped 44 pound package can be. On the other hand, all the essential peripherals are integrated into the unit, and all you need is a wall socket to power up and start typing in BASIC programs.

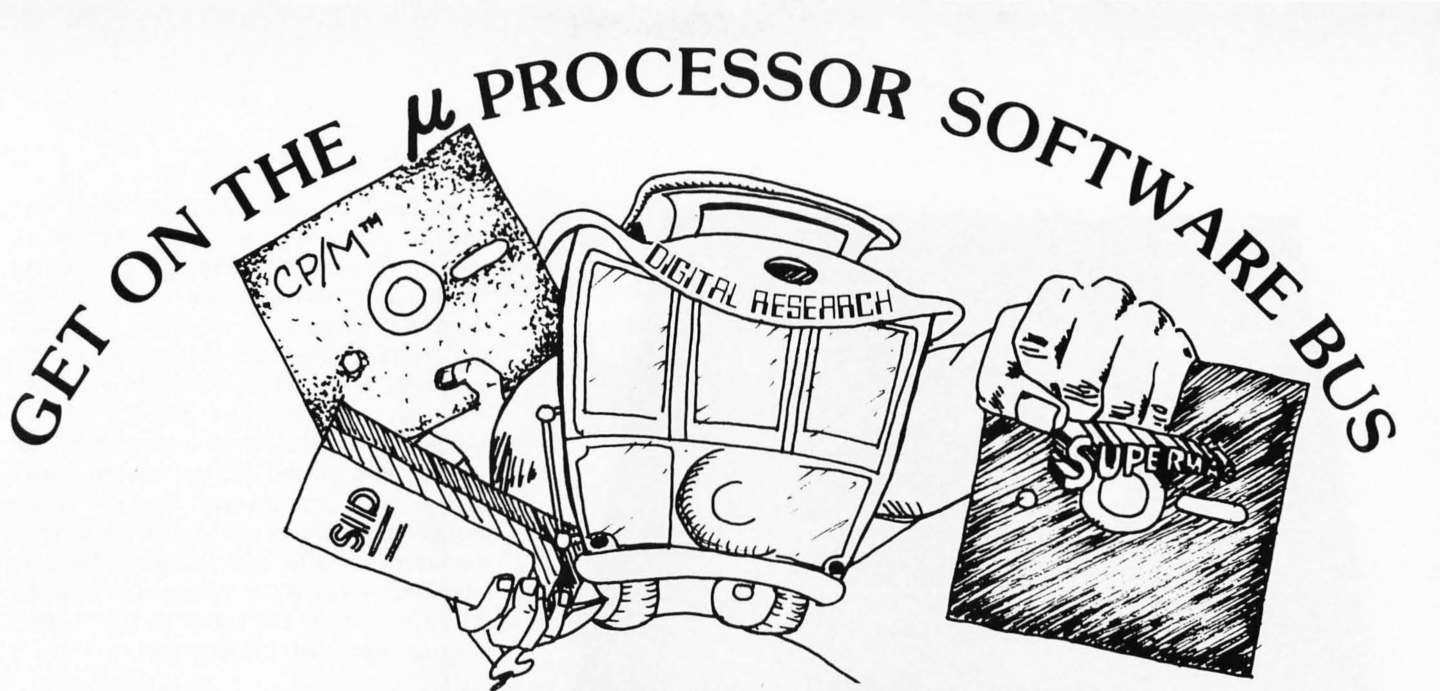
A powerful BASIC interpreter and an operating system presently supporting multiple external peripherals are built into the PET's 14 K bytes of read only memory. The basic PET for $595 includes an additional 4 K bytes of programmable memory, which holds your currently running BASIC program and data. An expanded model for $795 includes 8 K bytes of user memory (the maximum amount of memory inside the standard cabinet). Thanks to the efficient encoding of BASIC statements (see below), even the basic 4 K unit can hold up to a few hundred lines of program text.

Since Commodore had acquired MOS Technology Inc as a captive source of its calculator chips and other silicon requirements, the PET is based on the MOS Technology 6502 microprocessor. This may not be of much significance to the casual user since the machine is primarily designed to be programmed in BASIC, but it may make a difference to the experienced hobbyist who intends to write machine or assembly language programs as well.

Display Screen

The PET includes a 9 inch (22.9 cm) enclosed, black and white, high resolution CRT display which presents 1000 characters, arranged in 25 lines of 40 characters each. The display is memory mapped (ie: continuously read out of a section of programmable memory separate from the BASIC program and data memory), and is easily controlled from BASIC using PRINT and POKE statements. (PET owners who have not already done so may want to experiment with direct access, via POKE statements, to the display memory, which starts at location 32768.)

Built-in software provides a winking cursor and automatic scrolling from the bottom of the display. The cursor can also be moved



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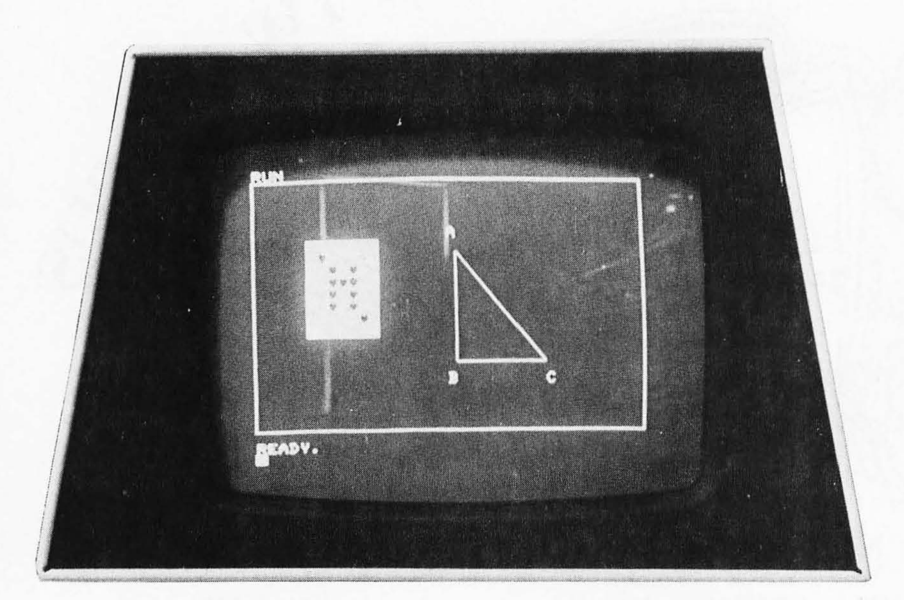


Photo 3: A simple example of the PET's graphic capabilities. This display was created with a series of 23 BASIC PRINT statements. The graphics characters in each character position run together to form the figures. The playing card illustrates the use of the reverse field option.

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in any direction using the cursor control keys (see the keyboard layout shown in photo 2), and the insert/delete key can be used to "push apart" characters on a line to make room for changes or to delete characters and "close up" the space which they formerly occupied. These features provide a convenient way to modify a BASIC program without having to retype entire lines: just list the lines on the display, use the cursor control and insert/delete keys to make changes directly on the display, and press the return key after each line is satisfactorily modified. A key is also provided to clear the screen or to send the cursor to the "home" position (upper left-hand corner).

Character Set

The PET's standard character set includes 64 upper case alphabetic, numeric and special characters, and 64 graphic characters, which are generated by pressing the shift key and one of the regular character keys (see photo 2). Each character is formed on the screen in an 8 by 8 dot matrix, and each character position on the screen is contiguous to those around it, so that graphic characters can be run together to form lines, solid areas and other shapes and figures. Furthermore, a "reverse field" feature, applicable on a character by character basis, changes each white dot to black and each black dot to white. This in effect gives 64 additional graphic characters. Any of these characters, including the reverse field and cursor control characters, can be inserted into a BASIC language PRINT statement, so that interesting graphics effects can be created quite easily. A simple example of the PET's graphics capabilities is shown in photo 3. In general, the PET's graphics capabilities are better adapted for drawing pictures of this sort than for plotting mathematical functions.

For the person who is more interested in alphabetic text than in graphics capabilities, the PET provides an upper and lower case character set with a limited number of graphic characters. The lower case option, which is applicable to the entire screen at once, is enabled by means of a POKE statement which changes the setting of an address line on the character generator read only memory. The effect is to produce a lower case letter in place of the graphic character which normally appears when an alphabetic key is pressed in upper case shift. (Yes, you must press the shift key to get lower case, and omit the shift key to get upper case!) This is illustrated in photo 4.

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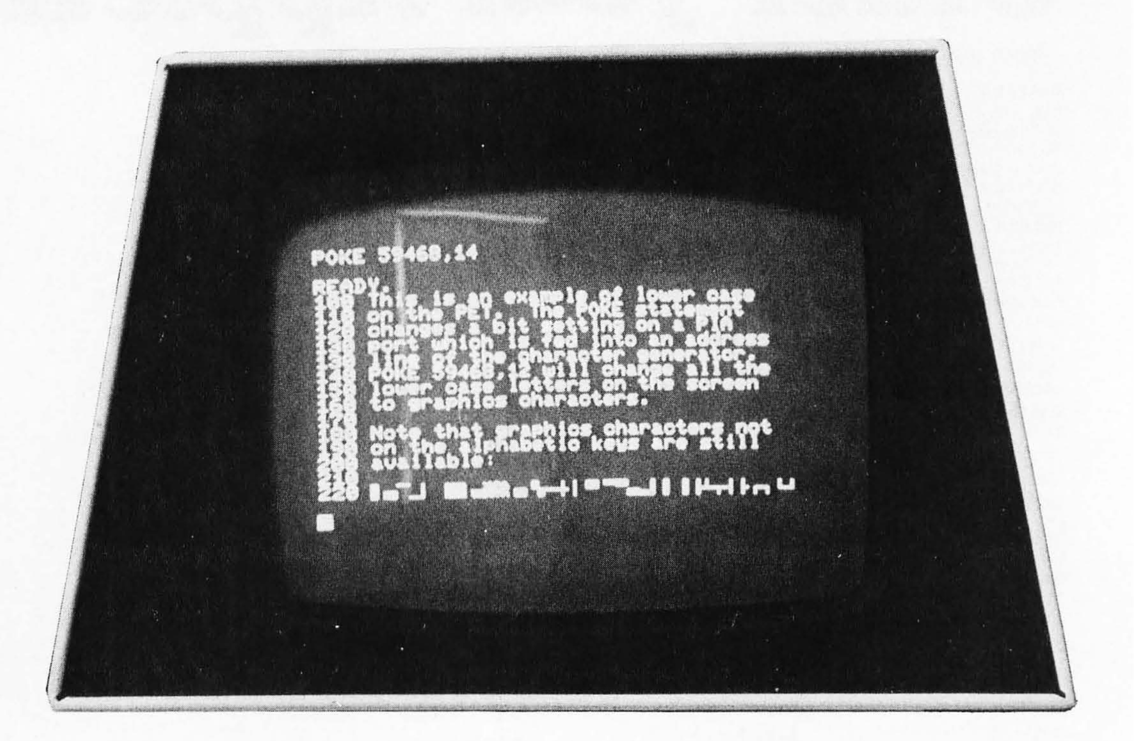


Photo 4: An illustration of upper and lower case letters on the PET. 26 of the 64 graphics characters can be exchanged for lower case letters by altering an address line on the character generator read only memory.

Keyboard

A much criticized feature of the PET is the design of the keyboard itself. It is a calculator style keyboard rather than a true typewriter keyboard. The keys are small and flat (about a half inch square and a quarter inch deep). They are tightly packed next to each other and are arranged in vertical rows rather than the slanting rows used on a typewriter keyboard. Although the alphabet follows the usual typewriter layout, the PET keyboard really cannot be used for touch typing because of the size, depth and spacing of the keys. The keyboard is said to be reliable and long lasting, but I did find that the space bar would not register correctly unless it was pressed squarely in the middle. Certainly the keyboard lowers the cost of the unit somewhat, and Commodore points out that their keyboard provides a larger number of keys and hence more graphic characters, but it is definitely more difficult to use. As a result many personal computer users may try to interface a separate typewriter style ASCII keyboard to the PET.

A BASIC program can obtain input of numeric quantities and character strings from the keyboard using an INPUT statement. But Commodore BASIC also includes a GET statement, which allows the program to capture each key from the keyboard as it is pressed without the scanning, editing and conversion normally performed by the BASIC system on input. This feature makes it easy to implement interactive keyboard games.

Cassette Drive

Also built into the PET's cabinet is an audio cassette recorder, which can be used for saving and loading programs and data. This device is hand operated much like an ordinary cassette recorder, but the motor can be started and stopped under software control, and the state of the manual switches can be sensed to a limited extent by software (yet the PET will still try to save a program on cassette if you've pushed PLAY instead of PLAY and RECORD). The cassette drive is said to be "modified by Commodore for much higher reliability of recording and record retention." The exact recording method used by the PET is not yet documented, but it appears to operate at a speed in the range of 1000 to 1400 bits per second. Because all information is recorded redundantly, the effective data transfer rate is about half this much. But the redundant recording enables the PET to detect and correct many recording errors. In my experience, data storage on the PET cassette drive has been remarkably reliable and trouble free.

Operating System

An elegant cassette operating system in the built-in read only memory supports named tape files of both programs and data, with file names up to 80 characters long. A SAVE command writes a program onto a tape cassette, and the thoughtfully provided VERIFY command can then be used to reread the program from cas-

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sette and compare it to the program still in memory to verify that it was written successfully. This is an essential feature when dealing with audio cassettes, if only for the user's peace of mind. A LOAD command will search down the tape for a named program and then load it into memory. Similarly, a data file, written on tape from BASIC by means of OPEN, PRINT# and CLOSE statements, can be searched for and read by another BASIC program using OPEN and INPUT# statements.

With a little care, programs can be chained together: a program segment in memory can automatically load the next program segment from cassette and continue execution. I was able to do this by placing LOAD and GOTO statements (separated by a colon) on the same BASIC line; the old program segment seems to be completely erased and replaced by the newly loaded segment, but data values are preserved.

The PET's built-in operating system is capable of handling multiple cassette drives and apparently other peripheral devices as well. A second cassette drive interface is in fact included in the basic PET.

Commodore BASIC

Table 1 summarizes the features of the powerful BASIC interpreter built into the PET Commodore BASIC, developed by the folks at Microsoft who brought you Altair BASIC, features real numbers, integers and strings, multidimensional arrays, a full set of mathematical functions, and a variety of extensions for string handling, input and output on external peripherals and machine language access.

Commodore claims that the PET's BASIC is at least 20 percent faster than other microcomputer BASICs, and the tests which I have run support this claim. In addition, Commodore BASIC is efficient in its use of memory, for it encodes BASIC statements as they are entered so that keywords such as PRINT and INPUT occupy only one byte. Another feature which can save time and memory space, especially when large arrays are involved, is the use of integer variables (which occupy two bytes) in place of real variables (which require five bytes). Programs are also stored on cassette in encoded form. This speeds up the process of saving and loading programs, but makes it more difficult (especially in the absence of documentation) to enter BASIC programs from an external device such as an ASCII keyboard or a paper tape reader, or to write programs, such as macroprocessors, which must manipulate program text as data.

For readers unfamiliar with Altair BASIC, the PET's character string handling functions are worth mentioning. LEFT$, RIGHT$ and MID$ are used to extract a substring of specified length and position from a character string. LEN returns the length of a string, and VAL and STR$ convert numeric quantities to character string form and vice versa. ASC obtains the internal character code for a given character, and CHR$ converts a character code into a single character string for handling as such in BASIC.

Machine Language Access

The PET user is not restricted to working in BASIC, for the PET is designed to support entry and debugging of machine language programs, and even other languages and programming environments. The BASIC user can examine or modify any memory location with the PEEK and POKE statements, or call a machine language subroutine via the USR function. Some nonstandard IO devices can be handled with the aid of the

Data Types:	Real numbers (eg: A), integers (A%) and strings (A$) of up to 73 characters.			
Arrays:	Any number of arrays of reals, integers or strings with any number of dimensions.			
Precision:	Ten significant digits for real numbers.			
Speed:	Executes the loop 10 FOR I=1 TO 10000, 20 NEXT I in about 15 seconds.			
Statements:	LET	GOTO		DIM
	READ	IF . . . THEN		REM
	DATA	FOR . . . TO . . . STEP		DEF FN
	RESTORE	NEXT		RUN
	PRINT	GOSUB		CONT
	INPUT	RETURN		NEW
	GET	ON . . . GOTO		LIST
		ON . . . GOSUB		CLR
		STOP		
		END		
Operators:	=	=		AND
	+	< >		OR
	—	>=		NOT
	*	<=		
	/	>		
	↑	<		
Built-in Functions:	ABS	SIN	FRE	LEFT$
	INT	COS	TAB	RIGHT$
	RND	TAN	SPC	MID$
	SGN	ATN	POS	CHR$
		LOG	TI	ASC
		EXP	TI$	LEN
			ST	VAL
				STR$
Other Features:	SAVE	OPEN		PEEK
	LOAD	CLOSE		POKE
	VERIFY	PRINT#		USR
		INPUT#		SYS
		GET#		WAIT
				CMD

Table 1: A brief summary of the features and performance of Commodore BASIC. The BASIC interpreter was developed for Commodore by Microsoft Inc, Albuquerque NM, designers of the original Altair BASIC. According to Commodore's engineers, the PET's BASIC actually includes some additional features not documented in the preliminary users' manual, from which this information was taken.

WAIT statement, which repetitively tests a memory location (such as a PIA port) until specified bits are set. Finally, the SYS command can be used to transfer "complete control of the PET" to a machine language subsystem previously loaded into memory.

According to Commodore's engineers, it is possible to save and load machine language programs on cassette, and undoubtedly an assembler in read only memory will be offered some time in the future. A machine language monitor, similar to MOS Technology's TIM, but utilizing the PET's keyboard and video display, has been developed for the PET. It was originally intended to reside in the PET's read only memory, but was squeezed out by other software and is now loadable from cassette, according to the latest word I've heard. As of this writing, Commodore has not released the machine language monitor on cassette, nor any documentation describing its capabilities.

Expansion

One of the nicest aspects of the PET's design is the degree to which expansion provisions have been built into the basic unit. The main printed circuit board is connected by means of plugs to the keyboard, CRT and built-in cassette. It includes four edge connectors which reach the outside world through openings at the base of the PET's cabinet. These edge connectors provide:

1. A second cassette drive interface with read, write, motor control and sense lines.
2. An 8 bit programmable IO port, actually the unused portion of an MOS Technology MCS6522 Versatile Interface Adapter (VIA).
3. An instrument interface obeying the discipline of the IEEE 488-1975 standard.
4. The microprocessor's address, data and control buses.

Provision for expansion is built into the PET's read only memory operating system as well. The second cassette drive and the IEEE 488 instrument interface appear to be fully supported by BASIC through the OPEN, CLOSE, PRINT#, INPUT#, GET# and CMD statements. Use of the VIA port and the address, data and control buses may require some machine language programming, although much could be done with the PEEK, POKE and WAIT statements

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Photo 5: The PET props open for easy service access. Besides the main printed circuit board, the unit contains a TV chassis type circuit board and a third board in the cassette recorder.

in BASIC. Special programming could also take advantage of the VIA's peculiar serial IO capability. And theoretically, one could unplug the built-in keyboard from the main printed circuit board and plug in another keyboard and logic interface. Again, Commodore to date has not provided documentation of any of the expansion options, and I have not been able to test these features. But I did see the PET driving a programmable oscilloscope in a demonstration at a trade show last summer. For those interested, the IEEE 488 interface standard documentation can be obtained from the IEEE Service Center, 445 Hoes Ln, Piscataway NJ 08854, (201) 981-0060.

Application Software

No application programs were supplied with the PET I received, not even a demonstration cassette which I had requested. But many of the first PETs off the production line are being delivered to people who have purchased one with the idea of developing generally useful application programs. Commodore plans to reproduce and sell application programs through its dealers, offering royalties to the software developers. And if the PET follows the pattern of other personal computers, additional systems and application software are likely to be offered by independents as well. Many application programs in BASIC can be found in books and in the files of large scale computer systems. Some of these programs are copyrighted and most will require some modification to fit the features of Commodore BASIC, but far less effort should be required to adapt such existing programs than to write the programs from scratch.

The PET has considerable potential in schools and universities, and it appears that many of the currently active software developers are especially interested in educational applications. I would not be surprised to see the PET show up in classrooms and university computer centers across the country, taking the load off game program burdened timesharing systems, and spurring new courses and educational research projects.

Availability and Delivery

Initially Commodore followed a policy of "cash now, delivery later" which meant, in my case, delivery on October 11 1977 of a PET which I paid for in late June. This was nominally within Commodore's contractual obligation to deliver in 90 days. This situation should change, however, as Commodore builds up its manufacturing volume and works off the backlog of initial orders. As this is written, I have heard that a few dealers have demonstration units on display in their stores, and at least one dealer has begun accepting orders on credit cards. Someday you may be able to buy a PET at your local computer store and carry it home, but until then you should probably base your plans and expectations on "worst case" estimates of delivery time.

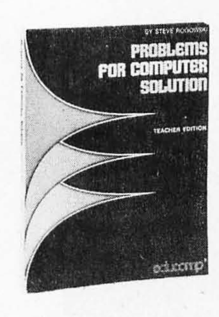
Warranty and Service

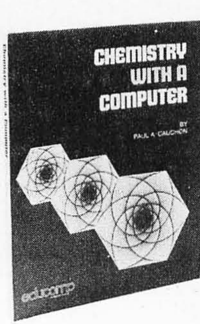
Service has always been a problem in the personal computer industry. It represents an even bigger problem for Commodore, since the PET will be distributed through calculator dealers as well as computer stores, to ordinary consumers as well as to computer hobbyists. Commodore's approach to the problem has been to design the unit to be serviced as easily as possible.

The PET cabinet props open for easy access, as shown in photo 5. The entire unit contains only three individually replaceable printed circuit boards. The main board can be snapped out and returned to the factory or replaced by a Commodore dealer. A 1 K byte diagnostic routine is included in the PET's read only memory,

Take a Byte of APL

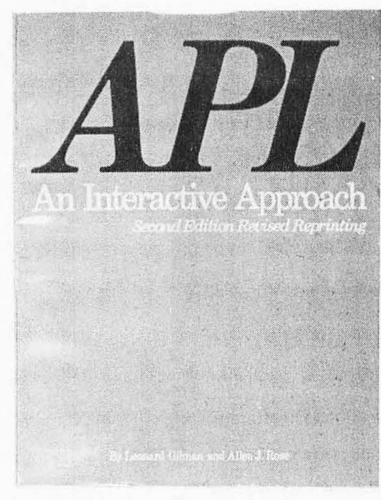
———**Problems for Computer Solution** by Steve Rogowski, Teacher Edition. A collection of mathematical problems designed to stimulate thought and encourage research by students towards the goal of a final solution. The subjects range from arithmetic through calculus and on to problems that have yet to be resolved. An analysis of each problem provides ideas on logical approaches to a solution, and a sample program demonstrates one possible final solution. $9.95.



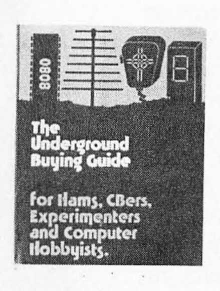


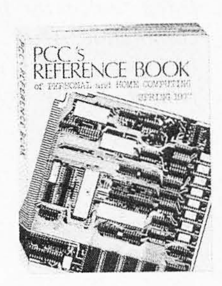
———**Chemistry with a Computer** by Paul A Cauchon. People are always looking for details of applications for the computer. It is one thing to say "gee whiz wouldn't it be nice if. . ." but such thoughts are but the stimulus to action. One result of a "gee whiz" idea is a series of educational and tutorial BASIC programs for use by teachers of chemistry, invented by Paul A Cauchon and published by Educomp Corporation. This book contains a collection of tutorial, simulation and problem generation programs which can be employed to advantage by teachers in high schools or colleges wherever a BASIC facility is available. If you're a chemistry professor or teacher by trade, or just a hobbyist interested in chemistry, this book will prove to be an invaluable tutorial aid. $9.95.

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———**The Underground Buying Guide**, by Dennis A King. Here at last is a source book for all those hard to find suppliers! It's designed especially for computer hobbyists, experimenters, hams and CB'ers, and can tell you where to buy items like connectors, discrete components, electronic music supplies, instrumentation, analog to digital and digital to analog converters, and synthesizers. The list goes on to include Teletypes, speakers, microcomputer software, cassette units, floppy disks and many other items. It will be an invaluable addition to your reference library. $5.95.





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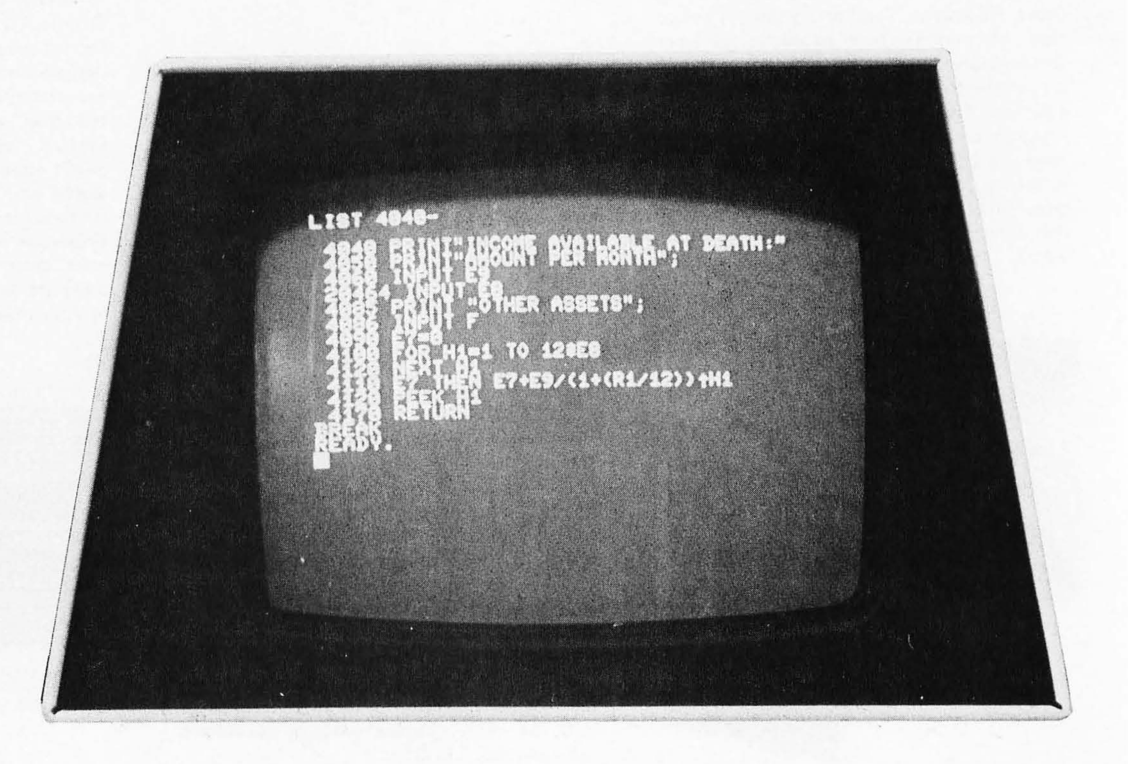


Photo 6: The PET received by the author was delivered with several faulty memory chips, which led to a variety of strange effects in BASIC as illustrated by this photo. The statement numbered 20464 was not typed by the user, and the statement numbered 4120 was listed twice by the LIST command. After the bad memory chips were replaced, these symptoms disappeared.

so that with special test equipment this board is "self-diagnosing." The second board, for the CRT display, is virtually identical to the same section of a chassis in a conventional TV set. The third board, for the cassette drive, is similar to the circuit board found in an ordinary audio cassette recorder.

Commodore believes that the PET could be serviced by a TV repairman equipped with a brief service manual. It is not yet clear, however, just how or whether TV repairmen might be licensed to repair PETs under warranty. Presumably experienced computer hobbyists could read the service manual and diagnose problems with their own PETs, requesting replacement parts from the factory, but how Commodore might react to this possibility is an open question. Of course, there is always the problem of latent bugs in the read only memory software, which a TV repairman might have some trouble diagnosing. Seriously, the only realistic approach to handling software problems is for hobbyists and PET dealers to document carefully with examples any anomalous behavior of their PETs, referring the information back to the software developers.

At present, however, PETs are being serviced only at Commodore's headquarters in Palo Alto CA. The user must arrange to ship the unit to Palo Alto and must be prepared to wait up to eight weeks for the PET to be fixed.

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Photo 7: *The Commodore PET 2001 is an eminently usable machine, as is illustrated by this display of a 6502 assembler written in the machine's version of the BASIC language. This assembler was originally written in FORTRAN for use on large systems, and implementing it in BASIC was a relatively mechanical job of translating statements and typing them into the PET.*

Although eventually Commodore may have a nationwide service network for the PET, my informal service experience with the early unit which I received has been quite similar to that reported by owners of other personal computers. I was unlucky enough to receive a unit with three bad memory chips which caused a variety of strange effects such as those illustrated in photo 6. For several weeks after I received the PET I was unable to get anyone at Commodore on the phone and was left to fend for myself. I suspected a memory problem, but my memory test programs written in BASIC apparently were not exhaustive enough to locate the faults. Finally John Feagans, one of the designers of the PET, called me, quickly diagnosed the problem and mailed me a machine language memory diagnostic program and some replacement memory chips. With these aids I was able to find and replace the defective chips in a couple of hours.

Conclusion

The PET may well be an "appliance" computer, suitable for the most casual computer user or, with appropriate application software, for the average consumer. But it is also a powerful tool in the hands of an experienced computer hobbyist. The options and flexibility built into the PET, ranging from string handling and machine language access to the second cassette interface and the IEEE 488 bus, make it quite suitable for expansion and enhancement. As a small illustration, despite the problems I have had with my PET, I have been able to debug and put into use several thousand lines worth of BASIC programs. Among these is a 6502 assembler written in BASIC, a program of about 700 lines which I orginally wrote in FORTRAN for use on an IBM 360 and a DECsystem 10.

For the casual user, the PET is a very low cost computer which can be programmed easily in BASIC, for use in schools, for playing games and for fairly complex calculations in engineering, statistics and the like. A better keyboard, a disk and a reliable printer would make it suitable for some business applications. In fact, Commodore is said to be considering development of a PET II computer which would incorporate several of these features. Whether the PET evolves into a general-purpose computer with a variety of programming systems and peripherals will depend on Commodore's future moves and on the activity of PET owners.

The PET is far from the only alternative in the marketplace today, but it is a strong contender. If you are contemplating a purchase, you would do well to compare its features against other offerings, talk to owners of the PET and other computers, and think about what you really *want from a* personal computer. I hope that this review article will help you in your evaluation.■

Continued from page 14

In conclusion, I would like to say that his last point, that his program is logically correct, is valid. Inasmuch as the purpose of designing before programming is to produce a logically correct solution to a problem, Mr Higgins has done well, but he should have stopped there. From there on, top-down structured programming should have taken over.

Douglas Drury
31 Brookmount Rd
Toronto, Ontario
CANADA

A COMMENT ON C FOR THE DEC 10

In his article "C: A Language for Microprocessors?" in October 1977 BYTE, J Gregory Madden mentions rumors about a C compiler for the DEC-10. I would like to direct his attention to a technical report from MIT. That report is MAC TR-149, "A Portable Compiler for the Language C" by Alan Snyder, May 1975. The compiler described in this report exists on the PDP-10 and HIS-6000 compilers.

Paul Dietz
Dept of Computer Science
Cornell University
Ithaca NY 14850

WAIT AND C?

The article "C: A Language for Microprocessors?" by J Gregory Madden (October 1977 BYTE, page 130) was in most respects a well-written tutorial revealing the overall flavor of the language. However, as one of the implementors of a new C compiler for the DEC PDP-11, I would like to correct several important inaccuracies in the article.

Contrary to what is said on page 132, column 2, the method for changing the value of a variable in the calling function is *not* an "explicit exception to the call by value rule," but rather employs a pointer argument.

Structures may *not* appear as arguments or the returned value of a function as claimed on page 136, column 2; but pointers to structures may so appear.

In the structure declaration on page 136, column 2, the initialization section should appear *after* the structure-name, not before it.

This reader was also momentarily confused by the use of "equivalence" on page 134 to mean assignment of a new value to a variable (eg: x = x+1).

Mr Madden's astute judgment that the C language is appropriate for microprocessors will soon be vindicated. We at Yourdon have just completed a C compiler and suitable documentation for the DEC PDP-11 running under DEC's RSX-11 operating system, and we anticipate offering an Intel 8080 version in early 1978. It will soon be transplanted to other DEC systems, including RT-11 for LSI-11s. What should also make Mr Madden happy is that C compilers from Yourdon are implemented in the C language and produce optimized source code in assembler language for the host machine!

Carroll Zahn
Senior Staff Consultant
Yourdon Inc
1133 Av of the Americas
New York NY 10036

ALARMING SYSTEMS?

In reply to M Barlow's letter in November 1977 BYTE, a Universal Alarm Annunciator is available from S & T Systems. The basic annunciator system consists of a microprocessor based controller with 96 optically isolated inputs. Alarm indications are displayed on a video monitor with as many as 14 alarm indications displayed at any one time.

Options available include a dual drive floppy disk for storing action procedures, a printer to produce a hard copy record of activities, and a paper tape reader for loading alarm messages.

The system with the disk option sells for less than $14,000. More information can be obtained from S & T Systems, 1302 Fawn St, Tullahoma TN 37388.

Joe B Thompson
S & T Systems
1302 Fawn St
Tullahoma TN 37388

COMMENTS ON APL AND OTHER TOPICS—FROM MALAYSIA

I am one of your new readers. Every time I savour your many fine articles, I have only one regret, that I did not discover your magazine earlier.

I have been following the interest in APL as evidenced by other readers' letters. Might I venture a few of my opinions on the matter?

As for the matter of binary representation, I believe that the ASCII code has one spare bit. This would allow up to 128 additional characters. (Or have they been assigned functions I don't know of?) An extra "shift" key would control this eighth bit directly, allowing the use of existing keyboard encoders. I think that using this bit for cursor indication on some terminals is sheer waste.

I may be wrong, but wouldn't an 8 K EROM like the 2708 suffice to decode all characters unique to APL for the video display? It could be configured as 64 by 16 by 8 (character by row by column). I count 48 special characters including overstrikes, with room for more. Once a standard has been established and demand rises, then a mask programmed version is not too far off. This shouldn't set the hobbyist back more than $25, perhaps less, now that the nonerasable plastic versions are in the pipeline. I am neglecting "burn-

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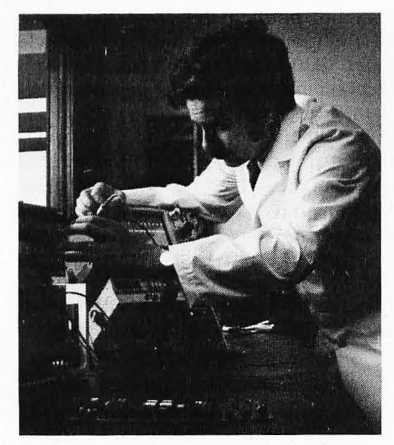
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ing" the PROM which is the labour of love anyway.

But whatever the final concensus, please let us have uniformity for the common good. Each setting up his or her own standard would only hinder the advancement of this lovely language on micros, not to mention problems of information interchange, etc.

I must confess that I am not praising APL from experience; I have access only to FORTRAN and BASIC. But from what I have learnt of it, I can't wait to get my hands on an APL terminal. Hassling with array manipulation in FORTRAN is really frustrating.

Keep up the good work!

Philip Yap Sue-Ken
4 Pesiaran Syed Putra
Kuala Lumpur 08-06 W MALAYSIA

MATHEMATICS SURVEY BY A READER

In the personal computer magazines I have read, I have not seen any reference to the practical role of mathematics in computing. Since I have had eight years experience in teaching college mathematics, and held an advanced degree in that subject, I find myself curious about this aspect. To do really well, do you need to know any more than how to punch the buttons on a cheap hand calculator?

This is not a question about what you need to get started: obviously all you need to get started is patience (lots of it), hard work and a willingness to learn. But does mathematics have a place in the growth and development of the hobbyist, and if so, how much of what kind? Are there specific situations where math was or would have been a big help? I am not limiting things to subjects of the traditional curriculum, but include things like binary arithmetic, Boolean algebra, model theory, statistics, etc.

In short, I am attempting to find out what hobbyists are doing (or not doing) with mathematics. I am preparing a questionnaire, which not only has a few questions but leaves a generous amount of space for comment on what is, what ought to be, or even on how stupid it is to fill out a questionnaire! I welcome any kind of response, including insults, so long as they are in good taste.

Bennett Sawey
318 N Maple St #16
Truth or Consequences NM 87901

I would wager that you will find mathematical concepts high on the list of "practical theory" embraced by many users of personal computers. . .CH

A COMMENT. . .

On page 174 of October 1977 BYTE, you pose the problem of determining whether two numbers A and B are nearly equal, to within some small range DELTA. You further specify that the

Circle 117 on inquiry card.

language in use has no absolute function, and then offer the horrendous solution:

```
IF ( (A-B)<0
    and (A-B)>DELTA)
or ( (A-B)>0
    and (A-B)<DELTA)
THEN . . . .
```

A much simpler solution is:

```
IF (A-B)<DELTA
    and (B-A)<DELTA
THEN . . . .
```

or the equivalent:

```
IF B>(A-DELTA)
    and B<(A+DELTA)
THEN . . . .
```

However, even shorter is:

```
IF (A-B)↑2<DELTA2
THEN . . . .
```

where DELTA2 is DELTA squared.

Incidentally, in floating point systems you never need an absolute value function if you have a square root function, since SQRT(A*A) will obtain ABS(A). The ABS function is a convenience, and in some systems may be less susceptible to roundoff.

H Bradford Thompson
Dept of Chemistry
The University of Toledo
Toledo OH 43606

But is your proposal any less a kluge? Extracting a square root — even with the best algorithm — has got to be a much more obscure calculation than the direct one given.

KOMPUUTAR UPDATES FROM DAVID BRADER

I have received questions from BYTE readers regarding my November 1977 article on "Kompuutar." Some of the questions are general enough to have a published reply for those who thought about writing but as yet have not.

About the 8 K byte dynamic memory. . . .The design is complete, but during debug I found that the $1 bargain chips I bought were not all functional. The board requires 16 IMS4060 or similiar chips, but only two have worked so far. Until I can afford to purchase 16 new (rather than used) memory chips, the project is halted. The design appears to function as intended but I will not publish or give out information until it is completely tested. I can say this much:

1. It is an 8 K dynamic memory system that is self-contained on one 4.5 by 6.5 inch (11.4 by 16.5 cm) vector card.
2. It refreshes itself invisibly to the rest of Kompuutar.
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4. It uses 4 K by one 22 pin TMS-4060 memories or similiar.
5. The cost (wire wrap model) with new chips is $180.

I have been asked about printed circuits for Kompuutar. I did a cost analysis of the system as designed (roughly $750 with 8 K of memory and a surplus multivoltage power supply), and then a time estimate for the printed circuit artwork. The results caused me to decide against putting out the effort for Kompuutar in its present form. I am considering some modifications to the design which will be upward compatible. If these work out over the next few months, I will reconsider committing Kompuutar to printed circuit boards.

Readers have frequently asked about software. The TIM chip has many subroutines which can be tapped if you are coding in assembly language. A 2.2 K byte Tiny BASIC is available from Microcomputer Associates in Santa Clara CA. Other software is advertised in publications such as BYTE.

Talking about TIM, people asked what will interface to it. Any ASCII serial input, ASCII serial output, or ASCII parallel input devices, such as: a Teletype ASR-33, HP 2644A terminal,

We've gathered the family to show you why PERCOM's™ Number 1 in cassette data systems for microcomputers.

Pardon us for doing a little boasting, but we're proud of our family. Proud of each member's reputation for performance and reliability. And pleased that we can offer the best in cassette data systems and data terminal interfacing at low, home-computing prices.

It took more than guts and a little luck to forge a position of leadership. We're number 1 because you get more when you buy PERCOM™. The reason, simply, is experience. Every product described in this ad is based on nearly 10 years of crucial involvement in the design and manufacture of computer peripherals that use cassettes for mass storage. Experience. It's why we developed a more reliable data cassette for home computing. Why our interfacing units provide **both** cassette and data terminal interfacing. Why you get the fastest, most reliable cassette data rates from PERCOM™. Experience. It's *the* reason for PERCOM™.

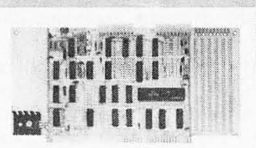


For your SS-50 bus computer — the CIS-30+

- Interface to data terminal and *two* cassette recorders with a unit only 1/10 the size of SWTP's AC-30.
- Select 30, 60, or 120 bytes per second cassette interfacing, 300, 600 or 1200 baud data terminal interfacing.
- Optional mod kits make CIS-30+ work with *any* microcomputer. (For MITS 680b, ask for Tech Memo TM-CIS-30+—09.)
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- Ordinary functions may be accomplished with 6800 Mikbug™ monitor.
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Prices include a comprehensive instruction manual. Also available: Test Cassette, Remote Control Kit (for program control of recorders), IC Socket Kit, MITS 680b mod documentation, Universal Adaptor Kit (converts CIS-30+ for use with any computer).

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For your S-100 computer — the CI-812

- Both cassette and data terminal interfacing on one S-100 bus PC board.
- Interfaces *two* recorders. Record and playback circuits are independent.
- Select 30, 60, 120, or 240 bytes per second cassette interfacing, 110 to 9600 baud data terminal interfacing.
- KC-Standard/Bi-Phase-M (double frequency) encoded cassette data. Dependable self-clocking operation.
- Optional firmware (2708 EPROM) Operating System available.
- Prices: kit, $99.95; assembled, $129.95.

Prices include a comprehensive instruction manual. In addition to the EPROM Operating System, a Test Cassette, Remote Control Kit (for program control of recorders), and an IC Socket Kit are also available.



For your data storage — Pilon-30™ data cassettes

- Orders-of-magnitude improvement in data integrity over ordinary audio cassettes.
- Pilon-coated pressure pad eliminates lint-producing felt pad of standard audio cassettes.
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PERCOM™ products may be purchased from home computer dealers nationwide, or may be ordered direct from the factory.*

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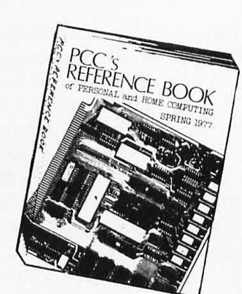
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PCC'S

Reference Book

of Personal

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Ever try to find the addresses of some manufacturers of, say, tape cassette or floppy disk interfaces for micros? Frustrating, isn't it? Well PCC has done something about it. This book lists hundreds of companies and stores selling hardware, software, and services. Survey articles on software, hardware, kits, applications and the future for the experienced and the not-so-experienced user of micros. Also included in this edition are bibliographies for further reference, book reviews, and an index of the articles from the major hobbyist magazines. All for the low price of $5.95, plus 50 cents postage.

Available through:



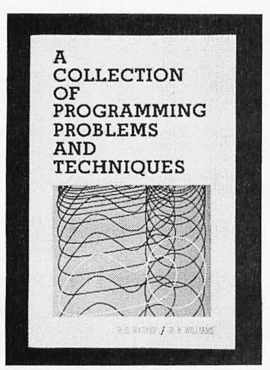


Master Charge and BankAmericard Welcome.

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Peterborough NH 03458

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—A Collection of Programming Problems and Techniques, by H A Maurer & M R Williams. Here's a book that presents you with problems! Nearly 400 of them, in fact: problems in games like chess, bridge, and NIM; practical problems such as applications of the law of sines, Cramer's rule for solving simultaneous equations, and applications of Latin squares to problems in probability; and more advanced computer science topics such as the use of Backus-Naur form. One quarter of the book is devoted to an appendix that gives stymied readers hints on how to proceed with solutions to the problems. The most valuable feature of the book, though, is its careful and thorough explanation of the use of algorithms to solve problems. No dyed-in-the-wool programmer or experimenter will be able to read this book for very long before trying to solve the tantalizing and well-presented problems. $13.95, plus 50 cents postage.



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Use coupon on page 147, writing in this books name.

a homebrew television keyboard terminal, high speed paper tape reader, etc, etc....

Having worked in the digital electronics area for several years, I took it for granted that anyone could get the parts that I could. I goofed! I have gotten letters requesting names of sources for some of the parts used in Kompuutar. This has caused two things to happen. One, I have tried to find a source for the "special" parts required. Two, I have tried to substitute more available parts in the design.

Two substitutions were decided on. The HP hexadecimal LED displays (HP 5082-7340) are replaced with TI L311 hexadecimal LED displays which are available and cost less. The Intel 3624-4 PROM is replaced by the Intel 2704 EROM. This second substitution impacts the power supply requirements and backplane wiring. With these two substitutions, I found that Jade Company of Lawndale CA (see advertisement in November 1977 BYTE, page 243) can supply all the ICs required, plus program the Intel 2704. I am sure other companies can also supply these items and recommend shopping around for the best prices.

The changes to the backplane and modifications to wiring, due to the substitutions, are available. For these and a helpful hints package, send $2 to the address below, to cover the cost of Xerox and mailing.

David Brader
Kompuutar Works Ink
POB 483
Electric City WA 99123

ON COMPUTERS AND DNA

Have you ever seen a computer reproduce itself? Well, neither have I, and that is the crucial difference between misapplication of computer technology and recombinant DNA research. If a computer gets out of the laboratory, it just sits there. If an organism gets out of the laboratory, it might just decide to have progeny, and if those progeny are pathogenic and can thrive, we're in trouble, big trouble. That's wherein lies the challenge of recombinant DNA. It's the only science that can implement itself without intervention of engineering. Think on that. That's where the threat is.

I'm writing in response, of course, to the letter by Mark Bizer in the December 1977 BYTE.

B J Luberoff PhD
Editor, *Chemtech*
The American Chemical Society
48 Maple St
Summit NJ 07901

Now That You Bring Up the Subject:

Politically, banning research in a given area will only drive the search for truth underground, witness a long series of historical martyrs to the under-

Circle 10 on inquiry card.

*standing of Nature starting with the Prometheus legend. The real dangers are unknown, in the same way that the dangers of atomic energy were unknown some 50 years or more in the past. But the potential benefits of genetic engineering make the risk well worth the challenge. . .*CH

RAMBLING RUMORS ABOUT TI

Recently, in San Diego CA, by one of those rare coincidences, I happened to fall into conversation with a person who introduced himself as a member of Texas Instruments' design section for pocket calculators. He has read BYTE from day one and was familiar with all TI matters therein, including my letter about the SR-51 working on the PC-100A printer.

It was a mellow evening and a pity I did not have a tape recorder and was not more alert in my questions to him. As for the SR-51 on the printer, some work and some do not. He said the SR-51A was primarily a repackaged SR-51 for cosmetic reasons. The printer itself has very little intelligence except for a character generator. The decision of what to print and where is a function of the calculator that is mounted on the printer.

As many of us know, the printer has very few moving parts: essentially a stepper motor that advances the rubber drive wheel for paper movement. The printer mechanism can be thought of as a single horizontal row of dots, although the row is actually staggered to aid in heat dissipation. Internal timing in the PC-100A compensates for the staggered dot positions. The stepper steps several times in order to work through one print line.

Q: Can the PC-100A be made into a portable printer to work off batteries away from a power socket?
A: Not likely because of the high current pulses required for its operation. The paper used in the PC-100A was purposely chosen to be insensitive for greater permanence. Note the cautions concerning sunlight and fluorescent light for some papers. Since the paper is insensitive, much greater heat is required. An incidental feature of the high heat is that the print head tends to stay clean when compared with other papers.

The answer to many of my questions was, "TI is a very aggressive company with the desire to make lots of money by filling the needs of the marketplace. When the bonafide need for a new product arises, if it is in TI's area of expertise, TI will be there, front and center," for example:

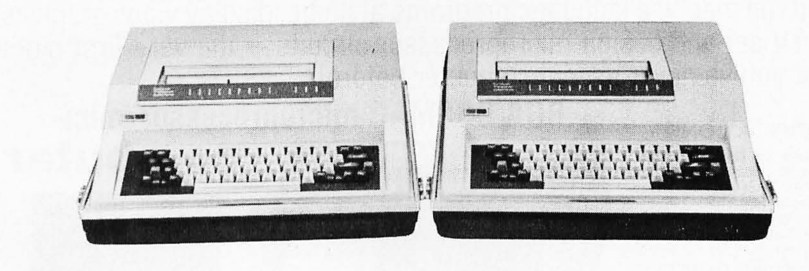
Q: What will TI do to enter the personal computer area?
A: It is a very aggressive company. . . .

One interesting tidbit from our long discussion is the fact that TI has used the same chip set in most of their recent pocket calculators of every sort. The processor in their new TI-59 is the same as was used in the old SR-50, and even the SR-50 was not the first use. The firmware and the firmware chips have varied greatly, and it is basically the firmware that determines overt functions and operations. When I asked why the TI-59 cannot compute a factorial, he said, "Oh, it *can* compute a factorial, but we needed the button for something else. The factorial is in the ROM of the chip, but you can't get at it."

Q: Will there be hidden gold on the TI-59?
A: Probably not. We worked our butts off to insure that all features are overt and well-documented. The TI-59 offers much more than the SR-52, hidden gold and all.

Q: Could you have given the TI-57 more than a mere 50 program steps?
A: Easily, but once again that was a marketing decision. More than 50 would have helped to compete, but it would

Can you tell our previously-owned **Execuport 300's** from our new ones? (No fair, peeking at the price.)



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have then also impacted the TI-58 and other TI calculators. In the total picture, including future pricing strategy, 50 program steps seemed right. The TI-57 is priced such that students can buy a calculator good enough for engineering use. The TI-57 does not suffer in comparisons until it is compared with calculators costing much more.

Q: Can you confirm the rumor that the calculator division of TI will eventually be as large as all other TI divisions put together?

A: TI is a very aggressive company. . . .

Q: Shall we have another round of drinks?

A: You are in very aggressive company . . . .YES.

San Diego is seldom foggy, but it got foggy that night.

Webb Simmons
1559 Alcala Pl
San Diego CA 92111

IT TALKS

The following unusual note appeared in our "in" basket on a "birth announcement" style greeting card.

FRIENDS —
AFTER 10 MONTHS OF HARD LABOR, I AM PLEASED TO ANNOUNCE THE BIRTH OF A BOUNCING BABY 6800; KNARF CAME ALIVE (?) TODAY*. MY TERMINAL HAD MANY DEFECTS AND WAS ALMOST ABORTED — BUT ALAS — WITH THE MIRACLES OF MODERN TECHNOLOGY — THE BABY TALKS AND LISTENS.

NAME KNARF
DATE DEC 11, 1977
WEIGHT ~15LBS, "N" OZ.
BORN TO FRANK DI GENOVA

BEST REGARDS, KEEP UP THE FINE WORK.
Frank DiGen

ON SOFTWARE PROTECTION

Mr Mirsich, in his "Opinion on Software and Patentability, 1977," November 1977 BYTE, page 162, is shortsighted in placing reliance on the law of trade secrets to protect "software" inventions.

The major use of microprocessors will be not in personal computers, but rather as logic replacements. Trade secret law will generally offer no protection against legitimate reverse engineering.

Consider, for example, a washing machine which, as a result of a new and nonobvious cycle sequence, provides an improvement over the prior art. Instead of implementing the new control with conventional logic, a microprocessor may be used instead. There is absolutely no reason why the new method of washing clothes, ie: the new machine cycle sequence, cannot or should not be protected by a patent. On the other hand, there is no way to "hide" the invention once it is embodied in the machine, and thus the law of trade secrets offers no hope for protection.

As for "software packages" sold in the form of tape cassettes, for example, it is true that patent protection is probably not available. But the law of trade secrets will be of equally little use. It is copyright protection which will probably be the best approach in such cases.

Michael I Rackman
Gottlieb, Rackman & Reisman
260 Madison Av
New York NY 10016

At BYTE, we put all our software eggs in the copyright basket.

AUDIO CASSETTE COURSES WANTED

Should you know of any institution or company offering microcomputer/microprocessor instruction on audio cassettes, please let us know.

Richard A Polacsek, MD
Director, Welch Medical Library
Johns Hopkins University
1900 E Monument St
Baltimore MD 21205

Can any readers supply this information? ■

HOBBYISTS! ENGINEERS! TECHNICIANS! STUDENTS!

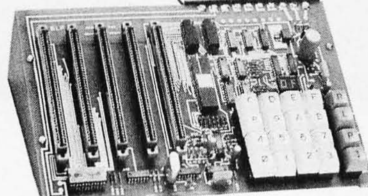
Write and run machine language programs at home, display video graphics on your TV set and design microprocessor circuits — the very first night — even if you've never used a computer before!

RCA COSMAC microprocessor/mini-computer

SPECIFICATIONS

ELF II features an RCA COSMAC COS/MOS 8-bit microprocessor addressable to 64k bytes with DMA, interrupt, 16 registers, ALU, 256 byte RAM, full hex keyboard, two digit hex output display, 5 slot plug-in expansion bus, stable crystal clock for timing purposes and a double-sided plated-through PC board plus RCA 1861 video IC to display any segment of memory on a video monitor or TV screen.

Use ELF II to ... **PLAY GAMES** using your TV for a video display ... **CREATE GRAPHICS** pictures, alphanumerics, animated effects ... learn how to **DESIGN CIRCUITS** using a microprocessor ... the possibilities are infinite!



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NOW AVAILABLE

ELF II explodes into a giant when you plug the GIANT BOARD™ into ELF's expansion bus. This powerful board includes cassette I/O, RS 232-C/TTY, 8-bit P I/O and system monitor/editor...meaning your ELF II is now the heart of a full-size system with unlimited computing power! $39.95 kit. $2 p&h.
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• Expansion Power Supply. $34.95 kit. $2 p&h.
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Yes! *I want to run programs at home and have enclosed:*
☐ **$99.95** plus $3 p&h for **RCA COSMAC ELF II kit. Featured in POPULAR ELECTRONICS.** Includes all components plus everything you need to write and run machine language programs plus the new Pixie chip that lets you display video graphics on your TV screen. Designed to give engineers practice in computer programming and microprocessor circuit design, ELF II is also perfect for college and college-bound students (who must understand computers for any engineering, scientific or business career). Easy instructions get you started right away, even if you've never used a computer before!

As your need for computing power grows, five card expansion bus (less connectors) allows memory expansion, program debugger/monitor, cassette I/O, A to D and D to A converters, PROM, ASCII keyboard inputs, controllers, etc. (soon to be available as kits). Manual includes instructions for assembly, testing, programming, video graphics and games *plus* how you can get ELF II User's Club bulletins. Kit can be assembled in a single evening and you'll still have time to run programs, including games, video graphics, controllers, etc., before going to bed! ☐ **$4.95** for 1.5 amp 6.3 VAC power supply, required for ELF II kit. ☐ **$5.00** for RCA 1802 User's Manual.

☐ **I want mine wired and tested with the power transformer and RCA 1802 User's Manual for $149.95 plus $3 p&h.**
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Let's Get Personal in Anaheim

June 6-8, 1978

A rewarding personal experience is in store for you June 6-8 at the NCC '78 Personal Computing Festival... the most comprehensive personal computing event ever held. The Festival, a separate feature of the National Computer Conference, will include approximately 30 program sessions, commercial exhibits of consumer computing products and services, plus a contest and exhibit of microprocessor systems and applications. All Festival activities will take place in the Disneyland Hotel Complex, just a few minutes from the Anaheim Convention Center, site of this year's NCC.

Plan now to attend the big, new NCC '78 Personal Computing Festival. The program will include special paper, panel, and tutorial sessions on such topics as speech synthesis and recognition, computerized music systems, hardware and software design, computer graphics, and small business systems. All papers will be published in a softbound volume, *Festival Digest '78*, which will be available during NCC.

Festival exhibits will provide an extensive display of commercial offerings by organizations serving the personal computing field. More than 100 companies, occupying over 175 booths, will display systems, components, terminals, software, kits, disc and tape cassettes, relevant publications, and related hobby items.

Rounding out the Festival will be a contest featuring microprocessor systems, devices, and applications ranging from home-brew DOS and graphics terminals to educational applications and computer games. Prizes will be awarded for the best exhibits.

Don't miss the year's most exciting personal computing event. For more information, return the coupon or call AFIPS at 201/391-9810.

☐ Please keep me up-to-date on Festival plans and activities.

☐ My company is interested in exhibiting at the Festival.

☐ Please send me information on the special NCC Travel Service.

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NCC '78 Personal Computing Festival

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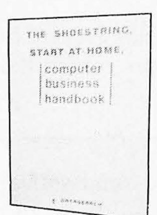


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21 START-AT-HOME COMPUTER BUSINESSES

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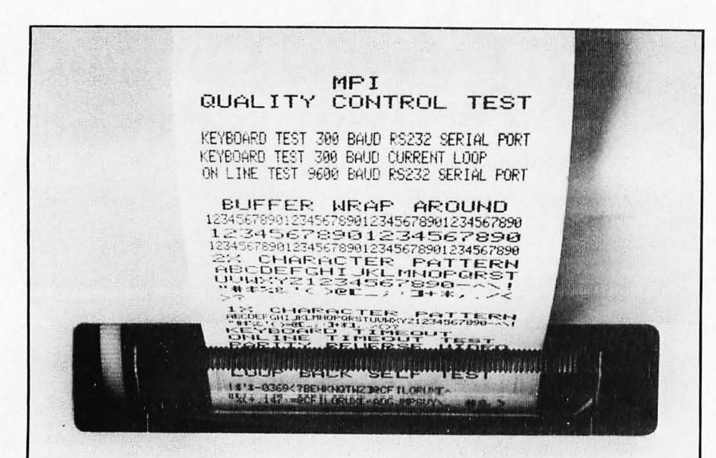
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Continued from page 6

The urge to solve the problem of automated editing tools with a small system has been growing within me for some time. Prior to starting this publication, I had often used the text editor of IBM's TSO software in preparation and testing of programs and job control in a large system timesharing environment. Earlier I had some experience with a more sophisticated editor, TECO on a DEC PDP-6. As a result of this experience, I dreamed of the possibility of a multiple window display, upper and lower case graphics, and lots of characters. Since then, as I found myself getting into word pushing with a vengeance as a daily way of life, the need for a practical approach to automated editing of manuscripts has become more important. I have seen examples of what a fast computer and good software can do in demonstrations of some automated editing tools used with PDP-10 hardware at Stanford Research Institute (now known as SRI International). Recently I have seen similar examples at Massachusetts Institute of Technology's Artificial Intelligence Laboratory. Ah, the frustration mounts! When would I find the time or money to duplicate such tools?

In many respects, I feel like the proverbial "shoemaker's child," running around "barefoot" with respect to the very technology about which I am most concerned. To be sure, I am a little hypocritical when I make this comment, for I do have a quite complete experimental laboratory in my basement: it currently has a loose federation of four different microcomputer systems talking to each other with programmed IO through parallel ports, each system specializing in a particular phase of the music control problems I spend my spare time upon. But this homebrew system is not a production tool for daily use in the office. Its status is anything but frozen, and as I experiment with the system it begins to resemble a bar of butter on a hot summer day. I am loath to use it as a production tool, for its very charter as a test bed for experiments is inconsistent with using it for regular work. Our present concept of automation in the editorial office has consisted of an IBM Correcting Selectric II typewriter on each editor's desk, the best electromechanical system, but far short of a computer text editing system.

Knowing full well that my personal homebrew system had limitations, I started a process of defining the requirements of a production text editing system which would fit my needs at the office and would be consistent with a "low" price tag using pro-

Circle 76 on inquiry card.

ducts drawn from the small systems field. It is in this activity of defining an editing system with as much standard hardware and software as I could get, that I found myself examining that class of complete systems characterized by extensive system software, extensive memory, video displays and mass storage on floppy disks. The activity of specifying such an editing system is the extent to which I have carried the search as of this writing in early December 1977. During 1978 I hope to see a practical fulfillment of this concept in one system. The result will not come up to the level of what I have seen at SRI in the way of high resolution displays and interactive text manipulation concepts, but I expect to get a workable and useful approximation at a price which I can afford. The requirements of the minimum system which will meet present goals are fairly simple to state:

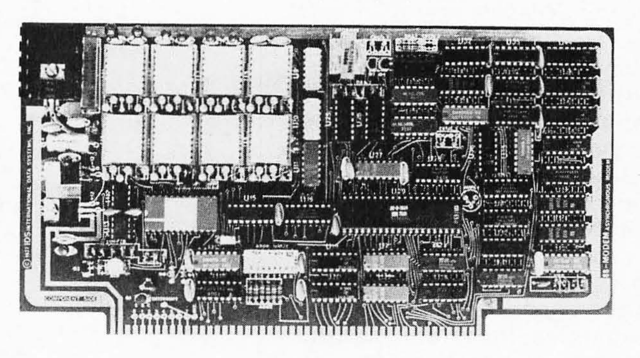
- The editing software must have a sophisticated programmable nature allowing definition and execution of macrooperations (with multiple levels of conditional execution).
- The editing hardware and software must support upper and lower case video displays with enough capacity to allow multiple simultaneous "windows" of information about the article file being edited. Initially, a command language oriented to an ASCII keyboard will suffice for interaction.
- The editing system must support software of a good floppy disk operating system with all the usual utilities, a macroassembler and one or more compilers.
- The editing system must read, convert, edit, reconvert and write IBM compatible EBCDIC text files on floppy disk media.

These requirements are based upon what I think I can get within the constraints of price (under $8000 to $10000 per system) and little or no software development or engineering design time on the part of myself and my associates at BYTE. Let's explore some of the reasons why these features might be important.

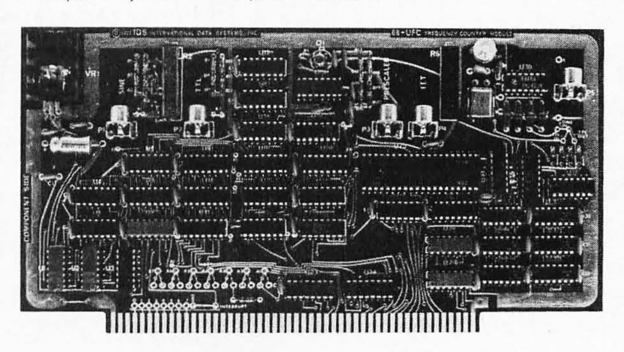
Programmable Editing. . .

As a individual thoroughly schooled in the uses and abuses of algorithms, one of my dearest wishes is to be able to specify procedures for the alteration of manuscript text, rather than mere "find" or "find and replace" or "delete" as found in most crude character oriented text editor programs.

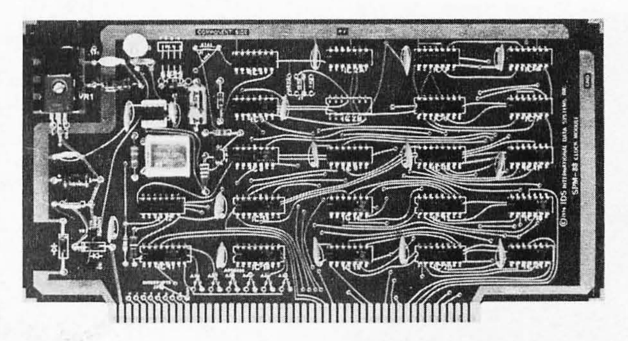
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Telephone (703) 536-7373



88-MODEM: A complete serial I/O port and an Originate/Answer MODEM on an S100 bus compatible board. The 88-MODEM features automatic auto-dialer (not software timed), operates at any software selected baud rate between 66 and 600 baud, has separate 8-pole transmit and receive active filters, and all functions are software selected. The 88-MODEM provides communication to -58 dbm and is intended for use with either a CBS (1001D) or CBT Data Access Arrangement for connection to the telephone system. The kit price is $245.00.



88-UFC UNIVERSAL FREQUENCY COUNTER: The 88-UFC is an S100 compatible frequency and period measurement module. The 88-UFC has four software selected inputs. Frequency measurement to above 600MHz and period measurement to 1/10th microsecond are standard. The counter provides nine digits of readout and is priced at $179.00 in kit form.



88-SPM CLOCK MODULE: The 88-SPM provides a time of day clock and an independent realtime clock on one S100 compatible module. Provisions are included for battery backup so the 88-SPM can maintain the time during power-off conditions. $96.00 kit

1001D (Type CBT) Data Access Arrangement	$125.00
88-RCB 16 Channel Relay Control Board Kit	$179.00
MCTK Morse Code Trainer/Keyer Kit	29.00
TSM Temperature Sensing Module Kit	24.00
DAC-8 8-Bit Digital to Analog Converter Kit	19.00
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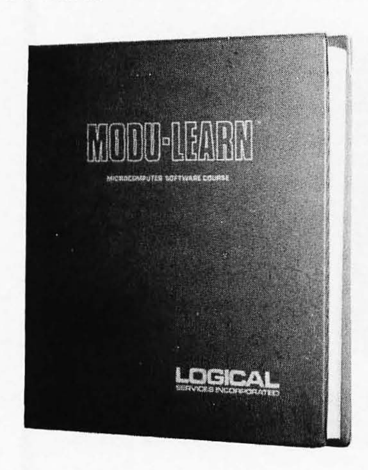
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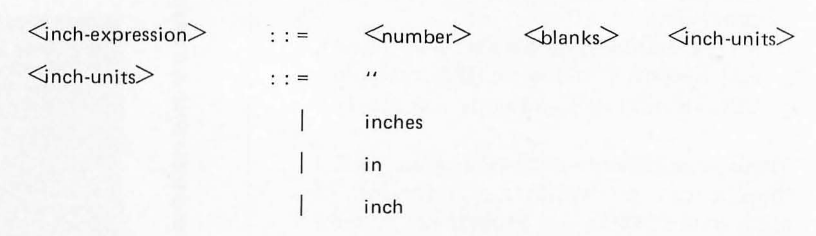
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As noted earlier, I was spoiled at one time in my life when I had about six months exposure to Digital Equipment Corporation's TECO text editor on a PDP-6 at the University of Rochester, Rochester NY. That taste was enough to convey the power of an editor in which I could compose conditional text alteration procedures, and execute them in real time to edit my files. (The files I was editing were a number of FORTRAN programs for John Conway's game of Life, implemented at the expense of my grades as a physics graduate student.)

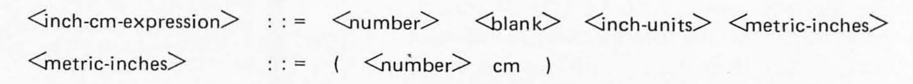
For those unfamiliar with TECO, which is still used in a number of forms on Digital Equipment Corporation's computers, all I can say is that it is addictive. I had no such feelings for the IBM TSO editor which I used later in my experiences, or for the quickly implemented and quite crude text editor I have since written for my homebrew system. The TECO I used six years ago has probably evolved considerably since I used it, but that one taste was enough to leave me in love with the method.

The idea of programmable character oriented text editing language is simple: the ability to program use of primitives for scanning text in search of matches to a syntax pattern, and conditionally modify the text based on local context. A classic example with which I deal all the time at a manual level is the case of a decimal number followed by zero or "n" blanks, then a double quote mark ("), or one or more variations of the abbreviations, and full spellings of the singular or plural form of the English language word "inch." In Backus-Naur form, this syntax might be noted:



```
<inch-expression>  ::=  <number>  <blanks>  <inch-units>
<inch-units>       ::=  "
                     |  inches
                     |  in
                     |  inch
```

The object of the macro to be composed for this case is recognition of this syntax or approximations of it, and replacing each instance with a standard representation of the measurement which includes metric equivalents calculated from the original English measurement. Ignoring the semantics of the transformation, the resulting syntax should be:



```
<inch-cm-expression>  ::=  <number>  <blank>  <inch-units>  <metric-inches>
<metric-inches>       ::=  (  <number>  cm  )
```

This "inches to centimeters" transformation

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is the prototype of a number of similar operations which convert any one of the usual English system units to metric within text. At present I do this manually with a pocket calculator featuring metric conversions, and a blue pencil for recording the results. With some ingenuity, a text editor of the sort I am looking for can probably handle most such conversions semiautomatically with interactive approval of the results during execution of the macro.

As frosting on the whole macro text editing capability, it would be most useful to record a library of symbolically referenced procedures such as "inches to centimeters" as they are developed, so that they can be called as needed through a simple sequence in the text editing command language. This may not be achievable through standard software which is used honoring the principle of "no software development" on my part.

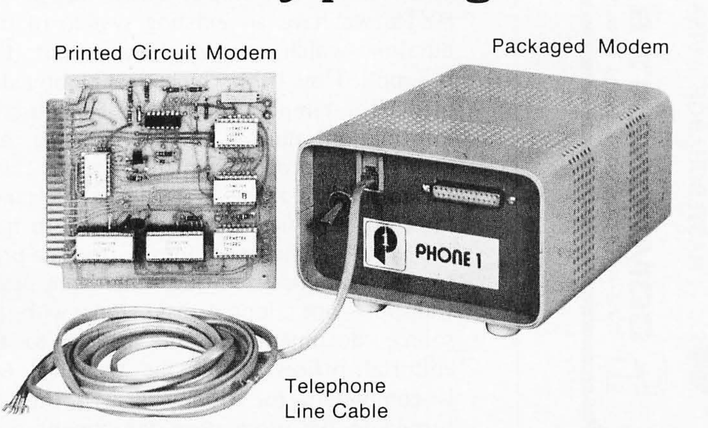
Capacious Upper and Lower Case Displays. . .

An editing system for manuscript materials without upper and lower case facilities is a contradiction in terms as far as I am concerned. One can certainly put up with upper case only text editing hardware in the context of any one of a number of existing high level languages and assemblers. But this absence of upper and lower case capabilities in such systems' software and hardware is an archiac carry-over from the earlier days of data processing and computing, when keypunches and Teletypes dominated the technology. The job of manuscript editing is impossible without a full upper and lower case capability. In judging articles for the magazine, I often will not accept a manuscript from an author which is typed upper case only, unless one or more exceptional conditions exist.

The use of video displays rather than hard copy is also crucial. I have no intention of waiting for a slow mechanism and creating mounds of waste paper as a result of the editng process. To be sure, hard copy will be used, but only in the form of a confirmation printout of the original state of the file supplied after the act of keying a manuscript to disk, and possibly as a final review of the results of the technical editing. An electronic display is essential to allow quickly scanning and examining details of text without the speed limitations of mechanical displays. The displays must be capacious also, since a mere 12 lines by 80 characters, or 16 lines by 80 characters, does not give a big enough field.

The ideal goal, which I have seen in the systems at the artificial intelligence laboratories mentioned earlier, is at least one full page of text, where a "full page" means perhaps 50 to 60 lines of text. This is the rough equivalent of the capacity of a page of single spaced typewritten copy. This capacity is then allocated to multiple logical windows on the data using the sytems software of the text editor. Such a display does not exist in any inexpensive practical form for the small system field, although it can of course be simulated. There are several Altair (S-100) bus products on the market which put up 24 or 25 line displays of 80 char-

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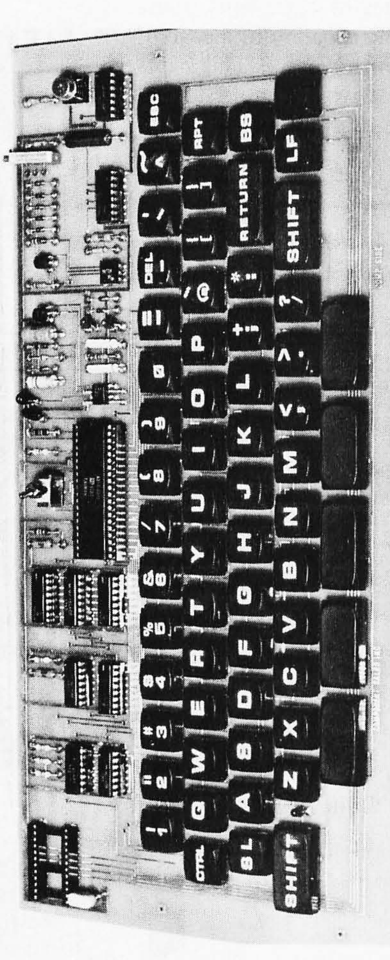
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acters; so if I purchase two such boards and two video monitors side by side vertically (or horizontally), I can come close to that design goal using standard off-the-shelf components.

The concept of assigning logical "windows" on the file's data is essential. In each article I edit, I have numerous categories of information which are logically separate, though related by belonging to the same entity. There is always the main body of text of the article; there is the captions list with subcategories based on the type of illustrative material being captioned; there is always a set of summary information such as the author's name, "about the author," the author's address, etc. There are sometimes additional optional materials such as glossaries, boxes of text which are auxiliary arguments not part of the main text, etc. Often it is necessary to scan one such logical subset of the article while retaining a segment of another such subset in view. For example, when checking a glossary item, the main text might be scanned while the glossary is maintained on the display. Or, when making a change of phrasing to clarify an author's point, the original text should remain on display while the modification is being made, just as I can always see the original text when I make pencil corrections in the manual method of editing. The ability to allocate multiple windows pointing to the same data set is only effective when the display area is big enough so that each window is of nontrivial size.

IBM Compatible Media. . .

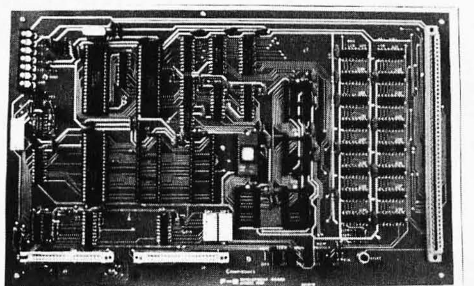
The requirement of IBM compatible floppy disk media is the only one which is driven by an external consideration specific to the context of BYTE publications. If the editing software were being used by an individual in an isolated situation, there might not be a need for either IBM compatibility or full size floppy disks. But here at BYTE we have an existing system of production which employs equipment that is supplied by IBM which uses floppy disk media for temporary storage of manuscript information during the typesetting and production process which happens after the technical editing of articles. The cleanest interface to this existing system is to have the input keying operations performed prior to the technical editing, then physically transport one floppy disk along with the source documents of the article to the editorial offices. After the technical edit is completed, the floppy disk is then returned to the production department along

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with the source documents, with all technical changes effected by the technical editors, rather than transcribed by production editors from penciled or typed corrections to a printed manuscript.

An Approach to Selecting Such a System's Hardware

With this rough functional description of what I want, how do I go about converting the idea into a working system with off-the-shelf hardware and software? This question is what caused me to begin a process of examining some of the more complete product offerings by various manufacturers which had the potential for meeting the required specification. The fact that I will even consider several of the former kit manufacturers for the personal computing marketplace as the principal suppliers is evidence of the maturity of this field as it has grown over the past few years.

My first and most important criterion is that the system must be purchased in complete form from one manufacturer (complete meaning "assembled, tested and demonstrated"). I do not want finger pointing (at least initially) due to conflicts over the ambiguous definitions of different manufacturers' hardware and software conventions. In my case, this will probably be accomplished by dealing directly with the manufacturer since we already have an established business relationship as a magazine; for readers of the magazine this can be accomplished by using a computer store as the local equivalent, with the proprietor selling a complete and working system demonstrated in the store before purchase. I may mix and match peripherals from other sources at a later time, but such

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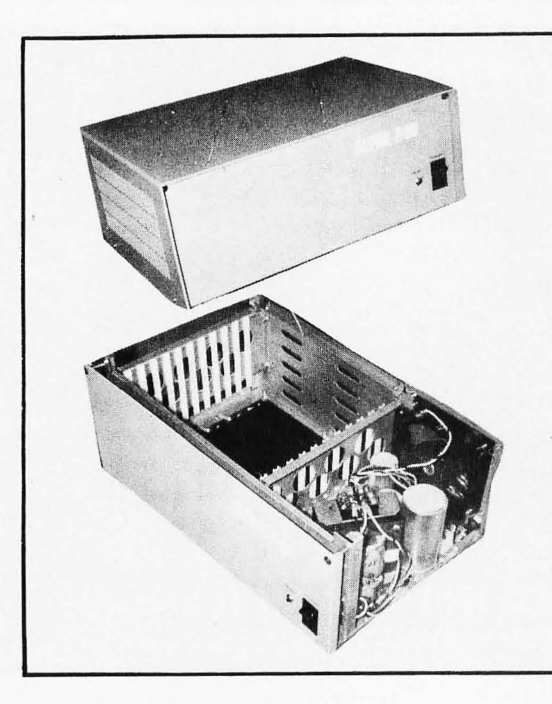
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incremental additions or modifications will only be done with the backup of a known working configuration.

The second and equally important criterion is that the supplier must be able to supply a complete set of systems software, already developed and operational, at the time of delivery of the system. This software includes a disk operating system, the text editor framework for the manuscript editing operations, and the usual macroassembler, linking loader and compilers of a "minicomputer-like" small system.

I highly recommend that potential users of a system either purchase or examine the manuals of the system they intend to buy, going over the manuals for purposes of evaluating completeness and quality of hardware and software support. In the past month or so, two examples of excellent documentation in a small computer system have come to my attention. One example is the so-called "preliminary" (but not very "preliminary" by most standards of documentation) manual of the Apple-II computer, discussed in the review appearing separately in this issue. A second example is provided by a system I am examining as a potential candidate for the editing function: the Technical Design Laboratories' Xitan product which has been seen publicly at a number of shows and computer stores. I recently travelled to New Jersey to visit TDL at the invitation of Roger Amidon. During that day long visit, aside from the usual rituals of visiting a company manufacturing for this field, I had opportunity to examine much of their software in operation, and to examine their version of a high capacity 80 by 25 character display with upper and lower case graphics. I picked up a pile of approximately 3 inch thickness filled with the excellent manuals for their software, which includes a FORTRAN IV with nearly complete ANSI features plus extensions, a macroassembler, CP/M by Digital Research as an optional operating system, a data base management system for the FORTRAN programmer called "MicroSEED," and the ZTEL text editing language which was the most important attraction of the trip. From the documentation, I was able to learn that much of the capability I would like to have for a text editing system used with manuscripts is likely to be available more or less off-the-shelf in ZTEL. There will be some custom work required, to be sure: for example, the editor does not support multiple editing windows, and will not be able to symbolically store debugged text editing macros on the floppy disk without some thought. But it may prove to be most of what I was looking for, especially with the use of two of the 80 character by 25 line display boards TDL is now manufacturing.

At the time of this writing, no decision has been made yet as to the details of such as editing system, nor have we purchased any equipment. I intend to review the manuals of a number of the manufacturers who offer good combinations of hardware and software which are potentially usable in this system concept before any final decision and purchase is made. But now that I have made the investment of reading the manuals, TDL seems to be a company which is well worth looking at.



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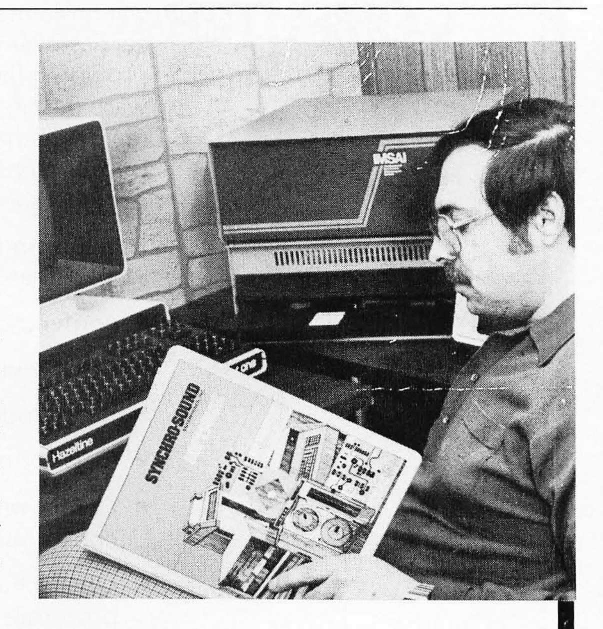
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Which Brings Me Back to My Original Point. . .

The theme which introduced this digression into editing hardware and software is that there are machines in existence right now, which are marketed as finished products, and which, with various degrees of software support, can be had at moderate prices in the $3000 to $8000 range through computer stores. This class of machines is what is needed to do "serious" personal computing. The characteristics of this class of machines, which has been maturing lately in the marketplace, might be given as: 16 K bytes of programmable memory and up, dual floppy disk drive, terminal, optionally some form of printer, and availability in a fully integrated form which needs no assembly from kits. Styles and configurations vary, of course, but the important point is that for the price of a good pickup truck, one gets a computer which can be effectively used for both utilitarian and frivolous computational uses at the whim of its owner. If the processor is an 8080 or Z-80, then Gary Kildall's CP/M operating system sold by Digital Research is frequently used with this kind of system, and often there is both a compiled high level language (for example TDL's or Cromemco's FORTRAN IV compilers) and a macroassembler. Rumor has it that PASCAL compilers exist which will be available shortly for this type of disk based system.■

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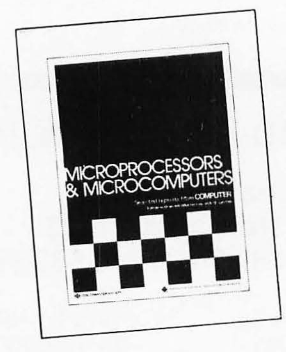
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32. Utilities, except power (telephone, telegraph, pipelines, etc.)
33. Distributor
34. School, university, or library
35. Others (explain)

JOB FUNCTIONS (Enter code) ____

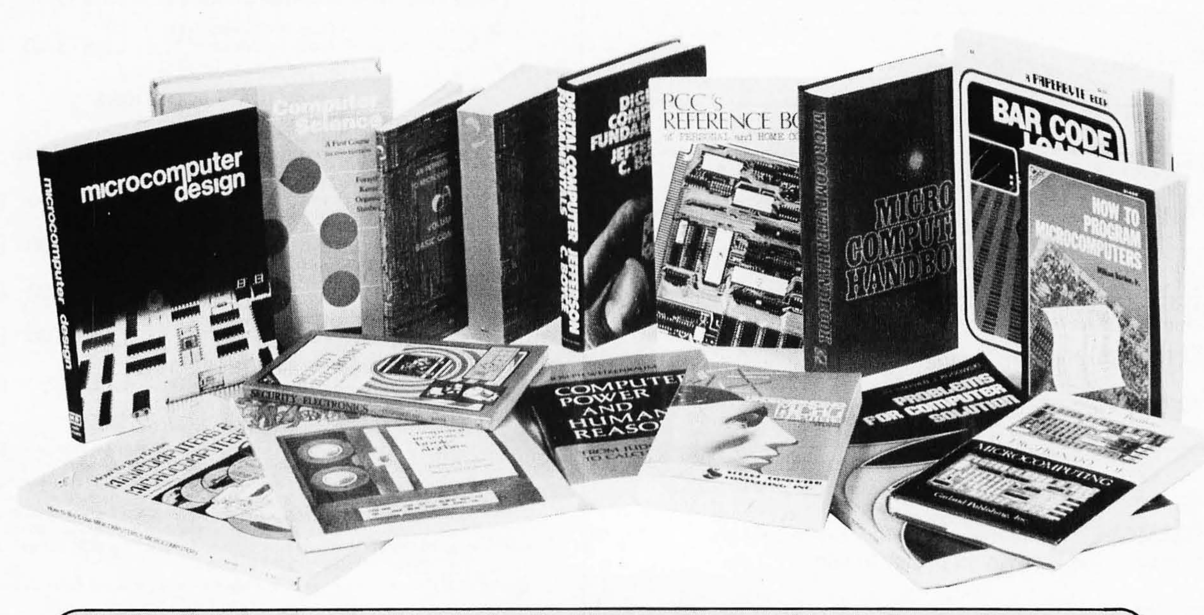
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4. Basic research
5. Manufacturing and production
6. Engineering support (draftsman, lab assistant, technician)
7. Purchasing and procurement
8. Marketing, including sales
9. Computer systems operations
10. Engineering systems planning and design (utilities)
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12. Dean, professor, instructor, etc.
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14. Other personnel (explain)

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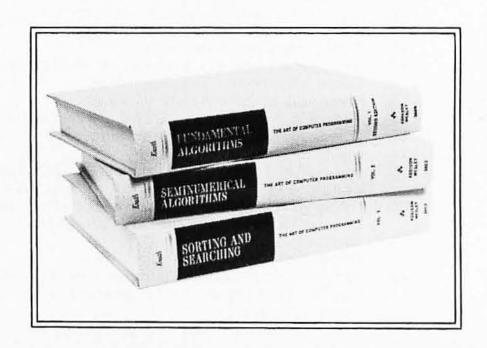
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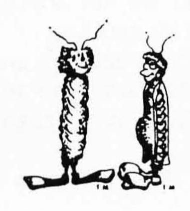
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The Altair (S-100) Bus Forum: PCC 77

John McCallum
Computer Science Dept
York University
Downsview, Ontario M3J IP3
CANADA

An Altair (S-100) forum was held at Personal Computing 77 in Atlantic City NJ in August 1977. The forum, led by William Goble, dealt with some of the problems of, and the future of the Altair (S-100) bus structure. As secretary for the group, I have tried to collect the ideas from the forum. I have also taken some liberties in adding additional information gathered at PCC 77 relating to the discussions.

Expansion of the Bus

1. Eight extra lines are not available on the bus for a 16 bit data bus.
2. 16 standard address lines are available plus four semistandard (A16 to A19) lines used by Technical Design Labs (TDL).
3. Expansion to a 16 bit data path can be achieved by:
   a. Ignoring conflicts on some Altair (S-100) lines, using them and ensuring your system will work (12 to 17, 59 to 66).
   b. Multiplexing data down the present data lines a byte at a time (the Alpha System does this, as does the 8080, etc, during a multibyte instruction): this entails a smart processor board. It *could* slow the processor timing *or* cause speed limitation problems with the bus. (This can also be used with 12 bit processors.)
   c. Using two parallel Altair (S-100) boards: a wasteful technique, but one which simplifies some problems.
   d. Using a ribbon connector on the top of the cards to connect extra data and address lines: this means that only the expanded precision cards are affected. Noise problems can be reduced in the connector by alternating ground lines and power lines with data and address lines. (32 data and 32 address lines would allow for any foreseeable expansion.)

Method b is most practical for immediate

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expansion. Method d is needed for long-range expansion for 32 bit microprocessors (perhaps as a 16 bit path used in conjunction with b to achieve 32 bits).

Problems with the Altair (S-100) Bus

1. Noise

   Two examples of bad Altair (S-100) bus layout were cited. The noise on these buses was such that intermittent operation of the system resulted. Noise on the bus can be caused by the following:

   a. Crosstalk

      Crosstalk occurs between adjacent lines along the length of the bus. The bus consists of the mother board *plus* the traces before ending at individual components on all boards in the system. High frequency signals are likely to be transferred from line to line. Spacing layout, construction materials of the mother board, and reflections (see next section) can all seriously affect crosstalk.

   b. Reflections

      When a signal reaches the end of the bus, part of the signal is reflected. [*Reflection can occur with any wavelike phenomenon, including light waves, sound waves, or high frequency electrical signals. It happens when the wave strikes a medium of different characteristics than the original medium (different density, for example, in the new medium).*] Reflection can be stopped by proper termination of the line. Two types of termination devices are in use in some Altair (S-100) bus designs. The effect of present terminators has not been studied in detail (even by the designers) to get comparative effects. However, the general consensus is that any attempt at termination is good.

2. Speed

   There is a limit to the Altair (S-100) bus's speed. This occurs due to a propagation delay of from 1 to 10 ns down the bus, and as a result of noise from reflection and the increase of crosstalk with speed. The speed limit changes with different design layouts. One manufacturer who had run computer simulations on their design would claim only 4 MHz with complete confidence (it was the cleanest system I saw). With at least two other systems running into trou-

Forum Attendees:

William M Goble
Jon E Avery
Michael L Shea
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Vincent Moscaritolo
Bing Huang
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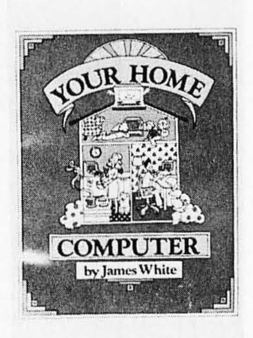
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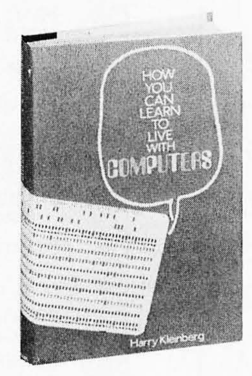
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bles even at 2 MHz, there is a real question of bus design and proper termination. Claims of some manufacturers with fast buses were in open question.

Conclusions were that if you have noise problems, add a terminator (terminator boards are available) and see what happens. On a well-designed system with proper termination and shielded layout of the mother board, the real speed limit should be about 10 MHz. On nonterminated unshielded systems, the speed limit will probably be about 3 MHz. Some study is needed to know more exactly, however.

3. Incompatibility

Several of the originally undefined pins have now been multiply defined (12, 13, 14, 56, 57, 58, 59, 60, 62, 63, 64, 65, 66, 67). These all have various definitions. There is no real way to correct or *prevent* these inconsistencies, since the individual designer can arbitrarily use the lines. For the user, however, we need to know the exact bus structure for each board so we can check for compatibility with our own systems. Thus *all Altair (S-100) bus products should include a bus description* showing which leads used on their individual boards are input, output, bidirectional, unused and speed (if clocks). A list of compatible and incompatible boards, and perhaps some outline of how to achieve compatibility would also be helpful.

In any case, the following de facto standard usage of lines is building up due to usage:

Pin 14	Battery backup (Seals, Ithaca Audio) (also being wired to top of board by most battery backup boards)	
Pin 60	A16 Address	(TDL)
Pin 61	A17	(TDL)
Pin 62	A18	(TDL)
Pin 63	A19	(TDL)
Pin 66	RFSH Refresh for dynamic memory (Z-80 systems) (Cromemco, SD Sales)	

4. Electrical

Some mention was made of government regulations and lack of shielding and interlock devices on boxes housing microprocessors. A question of UL approval of a device with different voltage sources on adjacent connectors was also raised. No one knows the status of the rumors, but it could cause problems for commercially packaged devices in the future.

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5. Duplication of data lines

With bidirectional bus drivers readily available, the use of eight extra lines for data in and data out is questionable. Some manufacturers are moving from data in and data out to bidirectional usage. This can cause difficulties in some designs of memory in a system. Although separate data in and data out lines cause inefficient use of space, there is some use in board design. Also, despite any inefficiencies, it is the standard; but on any bus *expansion* to 16 or 32 data lines, a bidirectional bus would be best.

General Comments

The Altair (S-100) bus has its problems. However, it is widely used (over 100 manufacturers produce products for it). It is speed limited, but then, the PDP-8 has not changed speed much in a decade. (The PDP-8 still compares well in benchmarks too!) Inconsistency in Altair (S-100) line definitions has usually caused few problems to users. Noise problems on the bus can usually be cleared up by adding termination or shielding, or by getting a new mother board. It has proved to be a workable basis for many design applications.

However, many designers will see its obvious faults and readily define a simpler bus, so we will see new buses in the future.■

REFERENCES

MITS, *Theory and Operations Manual—Altair 8800.*

D Denney and J Broom, "Why Not a Standard 100-Wire Bus Structure," *IEEE Computer,* October 1976, pages 57 to 58.

WM Goble, "Introducing the S-100: Standard Small Computer Bus Structure," *Interface Age*, June 1977, pages 66 to 79.

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CIE Net: A Design for a Network

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The CIE Protocols

Overview of the Protocols

Two kinds of protocols are needed to transmit messages from one CIE to the next. First the stations that want to talk to one another must agree on the language they will use for talking to one another, and second, the stations along the path between the two stations must agree on the language they will use among themselves for transmitting messages between the end points. For brevity, we can call the first one an end-to-end protocol and the second an interstation protocol. All these protocols share an important property that can be used to help them coexist with other non-CIE Net protocols, be they experimental variations or completely different protocols: each interstation transmission and each end-to-end message starts with a code that identifies the protocol set being used. In addition, each of the different end-to-end messages contains a crucially placed parameter line that identifies which (of a possible set of variations) is the appropriate way to interpret it.

The interstation protocol itself breaks down into two parts. When the stations first establish a connection, they must first negotiate the parameters they will use to initialize themselves. Once the stations are prepared to proceed, then they need a protocol that is adapted to the transmission of network traffic and additional interstation control information. For brevity, we will call the protocol in which the initial negotiations are transacted the initial connection protocol. Similarly, the protocol for transmitting interstation control information will be called the station control protocol. Since network messages will typically be so long that stations will generally wish to subdivide them into transmission blocks, we will call the main interstation protocol for handling network traffic the block framing protocol.

Most interstation traffic will be concerned with the transmission of network messages, so I propose optimizing the interstation protocol toward the block framing protocol in this fashion. When two stations are first connected, they will use the initial connection protocol to establish the parameters for all future conversations over the connection. The initial connection protocol is not very highly coded and so gains a very wide accessibility to a wide variety of protocol interpreters at the cost of inefficient utilization of the interstation channel. (Thus, the initial connection protocol can be used to establish the identity of the protocol set to a protocol interpreter that is prepared to handle protocols quite different from those I am proposing here. In fact, the initial connection protocol identifies itself in the first four characters transmitted over the connection.) At the end of the initial connection protocol, the stations agree to subsequently use the block framing protocol for all future transmissions. That protocol is quite highly coded for efficient utilization of the channel bandwidth and is optimized to handle transmission blocks of network messages; the station control protocol is

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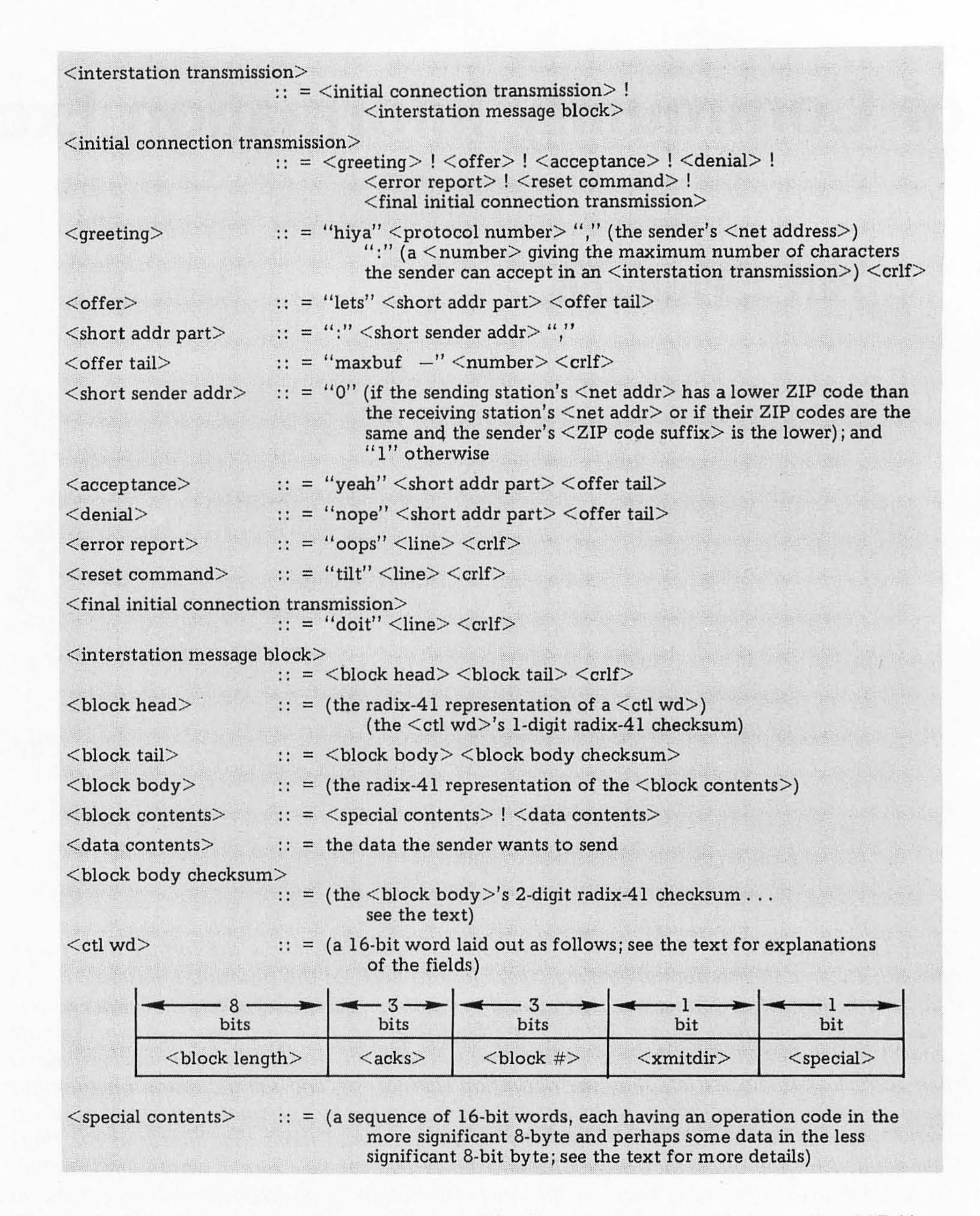
Part 2: Protocols

```
<BNF description>      :: = <equation> [ <BNF description> ]
<equation>             :: = <formal word> ":: =" <alternatives>
<formal word>          :: = "<" any text not including a right pointy bracket ">"
<alternatives>         :: = <sequence> [ "!" <alternatives> ]
<sequence>             :: = <item> [ <sequence> ]
<item>                 :: = <formal word> ! <informal description> !
                              <literal item> ! <optional item> !
                              "{ " <alternatives> " }"
<informal description> :: = any text (possibly including <formal word>s or <double quote>s
                              within parentheses), but otherwise including none of the (six)
                              brackets used in this definition, no exclamation point (nor any
                              <double quote>)
<literal item>         :: = <double quote> the text to be used (including no <double quote>s)
                              <double quote> !
                              a sequence (of three <double quotes>s) representing a single
                              (<double quote>)
<double quote>         :: = """"
<optional item>        :: = "[" <alternatives> "]"
```

Figure 1: Backus-Normal Form (BNF) Notation. I occasionally show the format of network messages, etc, in a slightly formal language very close to BNF. In this notation I present a bunch of equations that define formal words (enclosed in <pointy brackets>) in terms of other formal words, things that must appear literally in the thing being defined (enclosed in "double quotes") and informal English descriptions (not enclosed in anything at all). Each equation has a formal word on its left side, the definition sign (:: =), and the definition on the right side. A definition can include a list of alternatives (separated by exclamation points), of which exactly one must be chosen. Each alternative is a sequence of items that appear in the thing being defined (in the order they are indicated). Each item can be a formal word (whose definition is given in another equation), an informal description, a double-quoted literal item, an optional item (enclosed in [square brackets]) or a list of alternatives (enclosed in { curly brackets }). (Also note that, in spite of the fact that all literal items in my BNF definitions will be given in lower case, the distinction between upper and lower case is to be ignored. Thus, the literal "reply" should not be distinguished from "Reply," "REPLY" or "rePlY.") For example, my version of BNF can be defined by the above equations by using these same conventions.

handled by the block framing protocol as a special case.

The end-to-end protocol also breaks down into two parts. There is a common message frame, and there are five kinds of end-to-end messages that share it. The message frame shows, at the very least, the serial number of the protocol set in use and the address to which the message is being sent. It can also include some information for error detection, acknowledging intact receipt or both. The message frame can also include a unique identifier for the message. The five different types of messages are distinguished by a characteristic word just at the point where their formats diverge. Finally, the message frame provides for encryption, compression or segmentation of the message contents. Encryption is especially important if people are to trust the network to transmit their private messages through an unknown number of computers belonging to people whose intentions are unknown. Compression is provided just to economize the use of narrow channels. A uniform means of segmentation lets people



```
<interstation transmission>
                      :: = <initial connection transmission> !
                             <interstation message block>
<initial connection transmission>
                      :: = <greeting> ! <offer> ! <acceptance> ! <denial> !
                             <error report> ! <reset command> !
                             <final initial connection transmission>
<greeting>            :: = "hiya" <protocol number> "," (the sender's <net address>)
                             ":" (a <number> giving the maximum number of characters
                             the sender can accept in an <interstation transmission>) <crlf>
<offer>               :: = "lets" <short addr part> <offer tail>
<short addr part>     :: = ":" <short sender addr> ","
<offer tail>          :: = "maxbuf  —" <number> <crlf>
<short sender addr>   :: = "0" (if the sending station's <net addr> has a lower ZIP code than
                             the receiving station's <net addr> or if their ZIP codes are the
                             same and the sender's <ZIP code suffix> is the lower); and
                             "1" otherwise
<acceptance>          :: = "yeah" <short addr part> <offer tail>
<denial>              :: = "nope" <short addr part> <offer tail>
<error report>        :: = "oops" <line> <crlf>
<reset command>       :: = "tilt" <line> <crlf>
<final initial connection transmission>
                      :: = "doit" <line> <crlf>
<interstation message block>
                      :: = <block head> <block tail> <crlf>
<block head>          :: = (the radix-41 representation of a <ctl wd>)
                             (the <ctl wd>'s 1-digit radix-41 checksum)
<block tail>          :: = <block body> <block body checksum>
<block body>          :: = (the radix-41 representation of the <block contents>)
<block contents>      :: = <special contents> ! <data contents>
<data contents>       :: = the data the sender wants to send
<block body checksum>
                      :: = (the <block body>'s 2-digit radix-41 checksum . . .
                             see the text)
<ctl wd>              :: = (a 16-bit word laid out as follows; see the text for explanations
                             of the fields)
```

← 8 bits →	← 3 bits →	← 3 bits →	← 1 bit →	← 1 bit →
<block length>	<acks>	<block #>	<xmitdir>	<special>

```
<special contents>    :: = (a sequence of 16-bit words, each having an operation code in the
                             more significant 8-byte and perhaps some data in the less
                             significant 8-bit byte; see the text for more details)
```

Figure 2: Interstation transmission formats. The interstation transmissions of a CIE Net use the syntax of this definition. The two main components of the protocol are initial connection transmission used to negotiate parameters of initialization between the two stations, and the interstation message block or block framing protocol which is used for the bulk of network traffic. The design is optimized for the block framing protocol (end to end message frame), since this will be the predominant form of transmission on the network.

send files that are much longer than the network can gracefully handle as single messages. The five different kinds of messages sharing the message frame are:

- mail for people;
- file retrieval and storage;
- messages directed to other nets;
- messages containing or requesting statistical information; and
- replies to the other four classes of messages.

The Block Framing Protocol

The block framing protocol provides a number of features to ensure that messages are reliably transmitted between adjacent stations. (It bears some resemblance to the ARPA Net's Very Distant Host protocol and to a protocol known as DDCMP of Digital Equipment Corporation's DECnet.) It provides for error detection and retransmission. It provides for the proper sequencing of blocks in the face of lost or duplicate error-free transmissions. It will accommodate the half-duplex line discipline where it must, and it will capitalize on the full-duplex line discipline where it can. It uses the radix-41 representation for arbitrary binary data so that the programs that relay message blocks can be written in string BASIC. It also provides facilities to allow adjacent stations to test their connection and programs.

Message blocks have a format that is shown in figure 2. A block contains a head and a body; to provide error resistance on the telephone line, the head and body are each represented in a special radix-41 code (to be described in the third part of this series next month), and are separately protected by check digits. The block head has a 1 digit checksum, which is the sum (modulo 41) of the three (radix-41) digits representing it. The body, on the other hand, has a 2 digit checksum that makes the sums of the odd numbered (ie: first, third, fifth, etc) and even numbered (radix-41) digits of the <block tail> both zero. For example, if there are an odd number of digits in the <block body>, then the first <block body checksum> digit protects the even numbered <block body> digits. (Thus, the checksum calculation can proceed independently of the <block length>.) This interlacing helps resist noise that comes in bursts, as is most often the case with phone lines: noise is relatively unusual, but when it

Note: The third part of this series contains full bibliographic citations of selected cogent references, such as ARPA Net specifications.

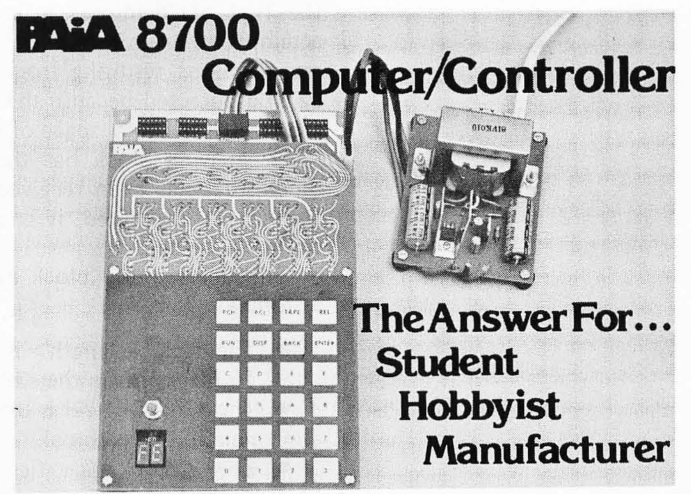
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occurs, it typically lasts long enough to wipe out several consecutive characters. With the transmission coded as several interlaced groups of digits that are separately protected, the chances are quite good that a burst of noise will be detected in at least one of the groups. Berlekamp observes that no error detecting code can resist more errors than can be represented by the check digits; two radix-41 check digits can detect 1681 of the possible error combinations. The particular scheme mentioned here is optimized to detect errors that are confined to two adjacent digits, but it can also detect isolated errrors.

Transmission blocks have numbers, assigned by counting (modulo 8) from zero; blocks going in each direction are numbered independently. Each transmission block includes its own number and the number of the next expected block in the other direction. Each station remembers the block number its partner most recently expected and takes care to get no more than four blocks ahead of its partner. Any arriving block that is in error is rejected, and thus treated just the same as lost transmissions. A station that has four unacknowledged blocks outstanding can then conclude that the first of them was in error and should attempt to retransmit it. The duplicate transmissions resulting from this procedure can be detected because the window is half the size of the total space of block numbers: if an arriving block has the number of a block that has been received since the last time it was expected, it is a duplicate and can be discarded.

The fields of a <block head>, then, are as follows:

- The <block length> is the number of 16 bit words in the <block contents>.
- The <acks> field is the number of the next expected block.
- The <block #> field contains the number of this transmission block.
- The <xmitdir> field is the <short sender addr>.
- The <special> flag is a 0 if the <block contents> are <data contents>, or a 1 if they are <special contents>.

A special block contains a number of 16 bit words that are used for maintaining the interstation link. They are distinguished by an operation code in the more significant 8 bit byte and can optionally contain data in the less significant 8 bit byte. They are:

0 — The message is complete, ie: the next data block starts a new message.

1 — Turn the line around. This one is used when the line is a half-duplex line, and so the stations must take turns transmitting.

2 — This block is just an acknowledgement; don't reply to it.

3 — I have buffers for some more data blocks; please send them. The number of data blocks that can be accommodated is given by the optional data and overrides all previous allocations.

4 — Goodbye, I'm signing off. Don't expect any more transmissions from me.

5 — Please reset yourself, I'd like to go back to the state of swapping <greeting>s.

6 — Echo this message, please, I'd like to see if it got to you OK. (Only the <block contents> are echoed.)

7 — This is the echo you requested. (All echo request bytes in the block are changed to echo reply bytes when the block is echoed.)

8 — Ignore the data part of this word.

9 — Something is wrong.

10 — Discard this block (but acknowledge it).

11 — Selective negative acknowledgement: the optional data part gives the number of a block whose head arrived intact but whose body did not.

12 — Ignore the <block #> of this block and process its <special contents> immediately. (This word must be the first in the <special contents> to assure proper processing of the block.)

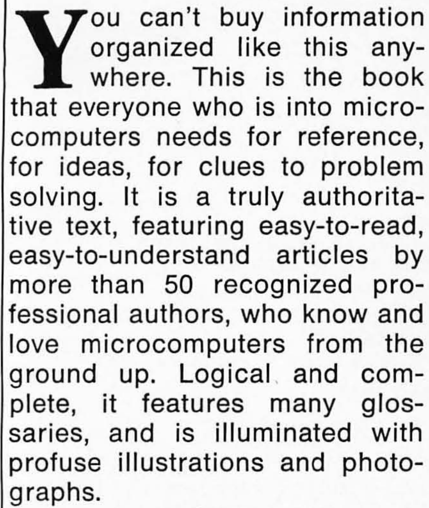
Note that these protocols say nothing about certain necessary operations. They are the steps by which the adjacent stations rendezvous and include operations like phoning a station's host computer, logging into its operating system and provoking the appropriate programs. The details of these operations are idiosyncratic to the host systems and cannot profitably be specified here. These protocols only cover the communications between the stations after their rendezvous has been established.

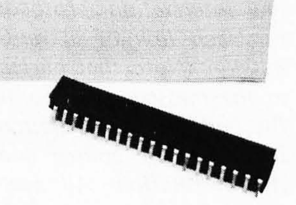
The End-to-End Protocol

The end-to-end protocol specifies that an end-to-end message consist of a uniform message header and one of five different kinds of message contents; the formats are shown in figure 3. In addition, the <message tail> (wherein resides the message contents) can be encrypted or compressed, or can contain only part of a long message. The <message head> contains all the informa-

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tion necessary for the automatic generation of replies in the reply protocol. Replies are at the option of the sending CIE. The first word of the <message tail> shows which of the five kinds of message tail it is, and the rest of the <message tail> is completely unspecified in top level of the end-to-end protocol. Otherwise, the first word of the <message tail> indicates that the tail is encrypted, compressed or partial, and a similar uniform format shows the true contents. Encrypted and compressed tails also contain a parameter line giving details of the procedure used, so that the source and destination of the message can agree on a number of alternative procedures.

It may not be obvious at first glance why message replies should be optional. Actually, there are two reasons, both of which derive from a desire to reduce network traffic by eliminating superfluous replies. Since the overall design for a CIE Net includes a very real possibility of lengthy transmission delays, the sending CIE may have lost interest in proper transmission of a message long before its reply arrives. Thus, the sending CIE is allowed the option of omitting any request for a reply just to simplify its own bookkeeping. On the other hand, many ARPA Net messages are sent that don't need replies on the lowest level either because they are acknowledged on a higher level, or

Figure 3: End to end message frame formats. This BNF text describes a syntax for data sent using the interstation protocol for each link of a transmission. Note that buried in the message protocol is the address information for both the source and the destination. All messages passed along the CIE Net are strings of data created according to this format.

```
<message>            :: = <message head> <message tail>
<message head>       :: = <protocol number> "," [ <message length> ":" <gap> ]
                              <dest net addr> [ <reply head> ] <crlf>
<protocol number>    :: = <number>
<message length>     :: = the number of characters (in the <message> expressed as a
                              <number> and counting each <crlf> as two characters)
<number>             :: = a decimal number
<crlf>               :: = a carriage return immediately followed by a line feed
<dest net addr>      :: = the address of the destination (expressed as a <net address>)
<net address>        :: = ["usa"] <gap> the ZIP code for the station's address "—"
                              <ZIP code suffix>
<gap>                :: = any sequence of zero or more tabs and blanks
<ZIP code suffix>    :: = a 3-digit number from 000 to 999 inclusive
<reply head>         :: = "(" [{"rsvp" ! "later"}":" <gap>] <source net addr>
                              [":" <message i.d.> ] ")"
<source net addr>    :: = the address of the message's sender (expressed as a
                              <net address>)
<message i.d.>       :: = <date>{"," ! " "} any text that (taken together with the
                              <source net addr> and the <date>) will uniquely identify
                              the (<message>) and that includes neither a carriage
                              return, a line feed nor a parenthesis
<date>               :: = the month (expressed as a <number>) "/"
                              the day (expressed as a <number>) "/"
                              the year (expressed as a <number> with two or four digits)
<message tail>       :: = <encrypted tail> ! <compressed? tail>
<encrypted tail>     :: = "crypt" <parameter line> <crlf> <compressed? tail>
<parameter line>     :: = parameters for the indicated process (expressed as a <line>)
<line>               :: = any text including neither a carriage return nor a line feed
<compressed? tail>   :: = <compressed tail> ! <partial? tail>
<compressed tail>    :: = "crunch" <parameter line> <crlf> <partial? tail>
<partial? tail>      :: = <partial tail> ! <real tail>
<partial tail>       :: = "partial (" <source net addr> ":" <message i.d.> ")"
                              {"section" <gap> <number> !
                              "bytes" <gap> <number> <gap>
                              "thru" <gap> <number> }
                              <gap> "of" <gap> <number> <crlf>
                              the indicated piece of a (<real tail>)
<real tail>          :: = <mail tail> ! <file tail> ! <reply tail> ! <stats tail> ! <gateway tail>
<reply tail>         :: = "reply"
                              [ "mail " ! "file " ! "reply " ! "stats " ! "gate "]
                              {"ok" ! "bad" ! "please" ! "unknown" ! "echo" ! "discard"}
                              ":" <gap> [ (the original message's
                              <source net addr> or <dest net addr>)]
                              (the original message's <message i.d.>)
                              <crlf> (any text)
<stats tail>         :: = "stats " any text
<gateway tail>       :: = "gate" any text
```

because the sender really cares very little whether they arrive at all. It would seem that, on the assumption that the same phenomemon will arise in a CIE Net, the sending process should be allowed to tell its CIE not to request a reply to be sent within the end-to-end protocol level. Note that a <reply head> containing a <message ID> must be included in a message for which a reply is expected at almost any level.

End-to-end messages should be arbitrarily limited in size to facilitate their transmission through volunteer relay stations and intermediate CIEs that are only loosely organized into a highly variable network. The consideration here is buffer allocation in the intermediate CIEs because they must handle whole messages rather than the smaller transmission blocks that are the concern of the relay stations. (Note that messages of any length can still be accommodated by several messages containing the appropriate <partial tail>s.) Probably the appropriate size would be somewhere between 1000 characters and 8000 characters; the lower limit is that of a single packet in the ARPA Net (which, according to Kleinrock, et al, can entirely contain 89% of the ARPA Net messages), and the upper limit is about the point at which operating systems begin to hassle their users. Message sizes in a CIE Net will probably be longer than in the ARPA Net because of the absence of the flurry of messages the ARPA Net needs to set up (and delete) the connection needed for the "real" message. The statistics of ARPA Net mail are probably a better indication of what to expect in the CIE Net: those messages typically run from 600 to 1400 characters. However, a CIE Net will probably contain a lot of messages that are even longer for two reasons. ARPA Net mail statistics exclude the transfer of files containing computer programs or extended documents; both of those tend to be longer than the installments of a running dialogue. Also, people who are relatively unfamiliar with the ARPA Net mail facilities tend to send messages that are 3000 to 8000 characters long, rather than the more usual shorter messages; those people are probably more representative of the participants in a CIE Net, at least when it first becomes operational. Thus, the standard maximum message size in a CIE Net should probably be somewhere between 5000 and 8000 characters.

The Mail Protocol

The mail protocol will look familiar if





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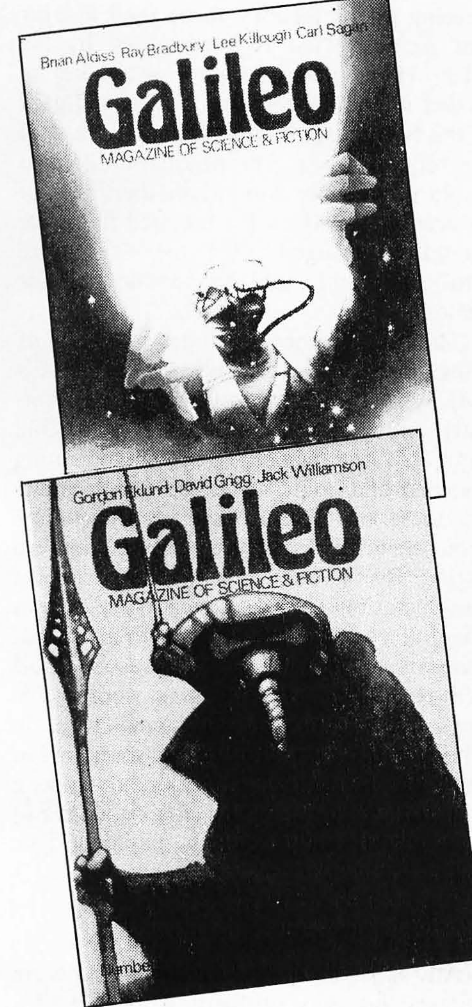
you know about the ARPA Net mail protocol. The protocol (see figure 4) is a compromise between the current ARPA Net mail protocol, its proposed replacement and the different requirements of a CIE Net. It specifies a <mail tail> to consist of a bunch of header lines, a blank line, and then the text of the mail. The header lines are intended to be intelligible both to a human and to an automatic message handling program; the text of the message is only intended to be intelligible to a human. The <user name> in a <mail address line> is intended to be a name that is intelligible to the appropriate destination CIE, and the <user name> in the <mail sender line> is intended to be intelligible to the sending CIE if a response is generated by a highly automated mail processing program. The only reservation is that a distinguished user name, *manager*, is to be reserved for mail sent to the people operating the CIE by people who don't know their names.

The header lines are grouped at the front of a mail message and are set off from the <mail body> by an empty line. The header lines are suggestively titled, but two of them should be explained somewhat further. The "from:" lines serve as signatures, and the "sender:" (or "sent-by:") line tells who actually sent the message; the <mail sender line> can start with "from:" if the person sending the message also signs it. The "enclosures:" line indicates the parts of the <mail body>; that can profitably be thought of as separate enclosures, such as other mail messages or files being forwarded. The <number>s are offsets into the <mail body>, with the first character of the <mail body> being numbered zero. Any enclosure whose end is implied by the beginning of the next enclosure or the end of the message can be indicated by a single number; other enclosures must be indicated by a hyphenated pair of numbers. Then, the automated mail systems have the information they need to help the recipient detach the enclosures. Any enclosure can, at the sender's option, be described by a parenthesized comment to further aid the recipient.

Figure 4: <mail tail> formats. Within the message frame protocol the type of message is determined by the type of tail applied to it. This <mail tail> enters the syntax of figure 3 as one of the options for a <real tail>. Mail messages contain the <mail body>, which is the message being sent, along with a variety of items specific to electronic mail activities carried over the net.

```
<mail tail>            :: = <mail head> <crlf> <mail body>
<mail head>            :: = "mail" <gap> <mail address lines>
                                <mail sender line>
                                [ <optional mail headers> ]
<mail address lines>   :: = <mail address line> [ <mail address lines> ]
<mail address line>    :: = { "to" ! "cc" ! "bcc" } <colon> <addresses> <crlf>
<colon>                :: = <gap> ":" <gap>
<addresses>            :: = { <individuals> ! <group> } [ ";" <addresses> ]
<individuals>          :: = <individual> [ "," <individuals> ]
<individual>           :: = <mailbox> [ "(" <personal name> ")" ]
<mailbox>              :: = <user name> { "@" ! <gap1> "at" <gap1> }
                                <net address>
<user name>            :: = <name>
<personal name>        :: = <name>
<gap1>                 :: = (a <gap> containing at least one character)
<group>                :: = <name> <colon> [ <individuals> ]
<name>                 :: = (any sequence of letters, digits, blanks, periods and dashes, but not
                                containing the string " at ")
<mail sender line>     :: = { "from" ! "sender" ! "sent-by" } <colon> <individual> <crlf>
<optional mail headers>
                       :: = <optional mail header> <crlf> [ <optional mail headers> ]
<optional mail header>
                       :: = <date header> ! <enclosure header> !
                                "in-reply-to" <colon> <source net addr> <colon> <message i.d.> !
                                { "from" ! "keywords" ! "password" !
                                "precedence" ! "authentication" !
                                (any sequence of letters and dashes not otherwise specified here for
                                the left end of a line in a <mail head> ) }
                                <colon> <line>
<date header>          :: = "date" <colon> { <date> ! <line> }
<enclosure header>     :: = "enclosures" <colon> <enclosure list>
<enclosure list>       :: = <enclosure item> [ "," <enclosure list> ]
<enclosure item>       :: = <gap> <number> [ "–" <number> ]
                                [ <gap> "(" <name> ")" ]
<mail body>            :: = the mail's body
```

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Large amounts of junk mail can be a real problem when the recipient must pay to store it for the time before examining it. There is, however, a partial solution that involves a novel use of passwords. A CIE could offer its users the option of splitting their file for incoming mail into two pieces, one having a negotiated maximum size and the other requiring a negotiated password for admittance. Then, an incoming mail message would be placed in the "goodguy" mail file if it included the proper password in its header; otherwise it would be placed in the junk mail file if there was room; otherwise it would be rejected. Presumably, people using such a facility would spread their goodguy mail password around and occasionally change it when it eventually spreads too far.

The most glaring flaw in this scheme is that a single energetic source of junk mail could prevent people from receiving legitimate mail from people who, for any of a large number of conceivable reasons, didn't happen to know the appropriate goodguy password.

The File Protocol

The file protocol illustrated is not too well thought out and should be taken as an extremely skeletal suggestion of what a file protocol should look like. Its main notable features are that it leaves file name format and user access assertion largely unspecified so that idiosyncrasies of diverse host systems can be accommodated gracefully. It allows a CIE to tell a second CIE to move a file to a third CIE in a manner similar to the DAP portion of the Digital Equipment Corporation's DECnet. Its most obvious shortcoming is that it treats files as indivisible atoms; perhaps it should also include a facility to subdivide a file like DECnet does. This would help conserve transmission bandwidth and buffer space by allowing people to selectively move small parts of files when appropriate. However, that would commit the <file tail> format to some particular file structure, and that commitment would be stronger than the commitments implicit in the <partial tail> or <enclosure item>. I omit that facility because it will be of limited utility at first, it is well-isolated from the rest of the protocols, it is highly arbitrary, and it can be added later.

One should note that the file protocol involves sending information (eg: passwords) through the net that, one might think, was better kept out of hands that are not completely trusted. That's not quite the case, however. Those passwords should more properly be thought of as very highly specialized tokens of limited utility. For example, a process requesting a file retrieval could arrange with its CIE for the storage of one file of a specified maximum size by file retrieval from a particular foreign CIE. Part of the negotiation would involve the file requesting process and the CIE agreeing on a password to be used just for that purpose (and then discarded by the CIE). Then, that password would be included in the file retrieval request and used in the file storage request it sends back with the requested file. The negotiation process would presumably also include the choice of an account to which the required file space should be charged; then the <file store info> wouldn't need to contain account names.

The file protocol includes a couple of things that can be idiosyncratic to the CIE's host system. The information (and its format) contained in <file access> and a <file name> varies widely between operating systems, and so it would be inappropriate for these protocols to say anything more about them than that they cannot contain a <crlf>. By the same token, a fair portion of the operating systems in captivity cannot gracefully append information to a file that preexists; a CIE with such a host should feel free to reject a file message whose <file store info> contains the "appe" verb. In other words, even though this specification gives the format of a request to append information to an extant file, it does not require that such requests be acceptable to all CIEs.

The Reply Protocol

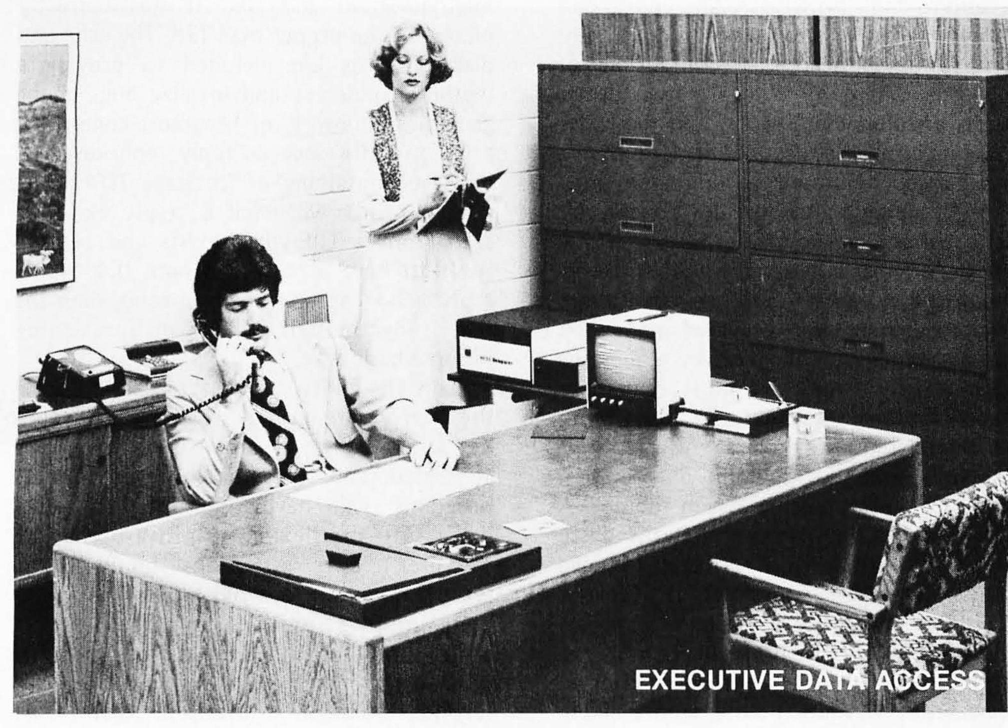
All replies in the end-to-end protocols are sent via the reply protocol. This is at variance with both the ARPA Net and DECnet, which extend each of their other protocols to include a separate idiosyncratic reply protocol. The reason for the difference is that both the other nets are oriented toward connections, over which flow many related messages, rather than being oriented toward the messages themselves. (Of course, the message orientation of a CIE Net is derived from the way it allows for very long transmission delays, which would require much longer connection lifetimes.) The <reply tail> can optionally include a word (eg: file) giving the general area of its relevance; it then contains more specific information on the disposition of the message for which it is replying or requesting a reply.

The reply protocol covers use of the <reply head> and the <reply tail>, whose formats are shown in figure 3. A <message>'s

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```
<file tail>          ::= "file" <line> <crlf> <file commands>
<file commands>      ::= <file retrieve> <crlf> [ <file commands> ]
                         ! <file store> <crlf>
<file retrieve>      ::= <file access> <crlf>
                         "retr" <gap> <file name> <crlf>
                         "dest" <net address> <crlf> <file store info>
<file access>        ::= "acce" <gap> (a <line> that will convince the recipient of this
                         <message> to grant the required access, typically containing
                         a subscriber name, password and account)
<file name>          ::= <line>
<file store info>    ::= <file access> <crlf> { "stor" ! "appe" } <file name>
<file store>         ::= <file store info> <crlf>
                         "data:" <line> <crlf> (the file's contents)
```

Figure 5: <file tail> formats. Another option for <real tail> in figure 3 is a <file tail>, used when the data sent in the end to end message frame is an arbitrary data file.

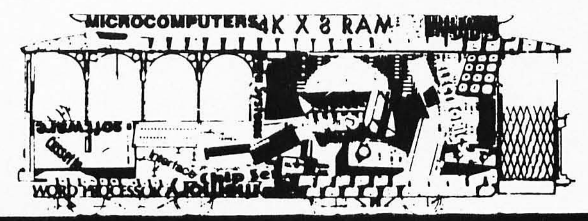
<reply head> gives it a "name," which it needs if it is ever to be acknowledged in the end-to-end protocol; it also provides a concise means by which an immediate reply can be requested at the top level of the end-to-end protocol. All end-to-end acknowledgements are carried in <reply tail>s. A <reply head> can contain one of the words "rsvp" or "later"; the former requests an immediate reply, and the latter merely informs the destination CIE that a reply may be requested at some later time.

A <reply tail> also provides a means by which replies can be requested at a time after the original <message> was sent. This part of the <reply head> is much more portentous than the previous paragraph indicates: when a CIE receives a message with a <reply head>, it must remember sufficient information to generate a reply upon a later request. Having sent a reply, it must still hold the relevant information against the reply's getting lost in the net. A <reply head>, then, means that the destination CIE must keep a *permanent* record of the <message> containing it! Clearly, that is too much to ask of any practical cheap CIE; the remedy is to permit the destination CIE to flush its records after an unspecified retention period, most likely ranging from a few milliseconds to a few weeks. If it is asked to reply to a message of which it has no memory, it can reply "unknown." Of course, end-to-end acknowledgement will be impractical for <message>s sent to a CIE with a very short retention period, but that is a matter more properly left for a CIE's subscribers to work out with the operators of their own and competing CIEs.

The <reply tail> also provides a means for replies to be sent from (or requested of) other levels in the end-to-end protocol; the optional qualifier (such as "file") gives that detail. Thus, an unqualified positive reply (ie: "reply ok") to a mail message needn't mean anything more than that the message arrived at the CIE and was dispatched to the program that handles mail. A positive reply qualified as coming from the mail program (ie: "reply mail ok"), however, necessarily means that it was intelligible to the mail program and that it was correctly placed in the proper mail file. The echo and discard verbs are included to provide a method to detect and localize bugs in the general framework of programs comprising a CIE; for instance a "reply reply discard" message containing a <message ID> in its <reply head> will elicit a "reply ok" message from a CIE that exists and believes itself to have a reply program. If a "reply reply echo" doesn't elicit an echo, then the reply program itself could be malfunctioning in some basic way.

This flexibility allows the user to *decide* the appropriate level at which replies should be generated or whether they should be generated at all. (Presumably the appropriate programs will have user interfaces that don't turn the flexibility into a burden on the user.) Two restrictions should be observed, however, to avoid loops. The first is quite intuitive: the reply to a "reply [xxx] echo" should be embedded in the appropriate type of "reply [xxx] ok" message. The second restriction is that all "reply [xxx] please" messages should refer to the original message of concern; if a "reply reply please" message inadvertently gets sent that doesn't refer to itself, then the receiving CIE should feel free to discard it without comment. Also note that a "reply [xxx] echo" message is the only one that can elicit a reply without itself containing a <message ID> in a <reply head>.

This completes the presentation of a sketch of a design for the communications protocols of a CIE Net. The BNF-like notation of figures 1 to 5 defines the grammar of the message protocols; some more of the dedetails of the design and its operation will provide the substance of the third and final part of this series next month.■





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Microchess 1.5 versus Dark Horse

Peter R Jennings
27 Firstbrooke Rd
Toronto, Ontario M4E 2L2
CANADA

When the Second World Computer Chess Championships were held in Toronto last August (see January 1978 BYTE, page 108), the opportunity arose to challenge one of the best chess programs in the world to a friendly match against my microcomputer. A match was arranged between Microchess version 1.5 and Dark Horse for the day after the tournament.

Dark Horse is a program written by Ulf Rathsman of Stockholm SWEDEN. It is written in FORTRAN IV and occupies 24 K words of programmable memory with 60 bit words on a CDC 6600 computer. On average, it is capable of analyzing 12,000 positions per move made. In addition, it utilizes its opponent's time by preparing replies to expected moves. Although Dark Horse is considered to be a small program by classical mainframe computer chess standards, its strategy is efficient and it finished in sixth place at the World Computer Chess Championships.

Microchess is a program I wrote for the

White: Microchess Black: Dark Horse

It was decided by a coin toss that Microchess would play white. Since neither program makes use of an opening book, the opening is a little unorthodox. However, by move 3 the position looks like a normal opening.

	White	Black
1.	N-QB3	P-K3
2.	N-KB3	N-QB3
3.	P-K4	N-KB3
4.	P-K5	N-KN5
5.	P-Q4	P-Q4
6.	B-KN5	B-K2
7.	BxB	QxB
8.	B-K2	Q-N5
9.	R-QN1	O-O
10.	P-QR3	Q-K2
11.	O-O	P-QN3
12.	P-QR4	Q-N5
13.	P-KN3	B-N2
14.	B-N5	P-QR3
15.	N-QR2	Q-QR4
16.	BxN	BxB
17.	P-N3	P-QN4
18.	Q-K1	QxQ
19.	R(B1)xQ	PxP
20.	N-N4	PxP
21.	NxB	PxP

Dark Horse evaluates the pawns captured plus the resultant pawn on the seventh rank as more valuable than the lost bishop.

	White	Black
22.	N-K2ch	K-R1
23.	R(N1)-B1	R(B1)-K1
24.	N-B6	K-N1
25.	RxP	P-QR4
26.	R(K1)-K2	P-R5
27.	N-N4	R(K1)-QB1
28.	R-N2	P-QB4
29.	N-Q3	P-R6
30.	R(N2)-Q2	PxP
31.	NxP	R-B5
32.	N-B4	P-R7

Dark Horse, which prints out the expected continuation, expected 33. RxP RxR, 34. RxR RxN, 35. R-K2, winning a knight for the pawn. It did not foresee 35. R-R8 (mate in one) because it truncated the analysis at 6 ply on this continuation. A search to 9 ply would be necessary to determine the threat.

	White	Black
33.	P-B3	. . .

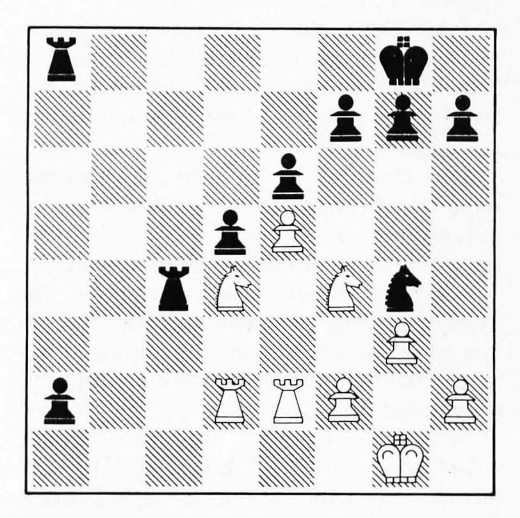
Microchess did not take the pawn because it expected the same continuation that Dark Horse projected, with the loss of a knight. The threat of P-R8ch was not evaluated correctly due to a bug in the program. This blunder resulted in a loss for Microchess.

	White	Black
33.	. . .	P-R8 (Q)ch
34.	K-N2	NxP (K5)
35.	N-N3	Q-B6
36.	K-R3	RxN
37.	PxR	QxPch
38.	K-R4	Q-N5 Mate!

Microchess took 47 minutes while Dark Horse required only 11 minutes of processor time for the game. Part of this difference is explained by Dark Horse's ability to compute responses on its opponent's time.

Although Microchess was defeated by Dark Horse, it was not as one-sided a game as might be expected given the difference in computing power. Further improvements in Microchess will probably bring it close to the playing level of Dark Horse and other programs in its class, but at a slower speed.

DARK HORSE



MICROCHESS

Position after 32. ... P-R7.

KIM-1 in 1976. Commercial versions are available for the KIM-1, and a translated version is available for the 8080. Version 1.5 is an extended version of the original program. It occupies 2.5 K of programmable memory and runs on a KIM-1 with expansion memory. Although it plays better chess than the first version of Microchess, it is incomplete and requires further development.

Because of the complexity of chess analysis, time becomes an important factor both for micro and mainframe programs. One expected solution to the problem is the use of multiple microprocessors to process portions of the analysis in parallel. Such a distributed network can reasonably be expected to play as well as Chess 4.6, if not better, provided the heuristics used are equally powerful. I would not be surprised to see this type of equipment in use at the Third World Computer Chess Championships in 1980 to be held in Tokyo and Melbourne.■

The following programs are available from Micro-Ware Ltd, 27 Firstbrooke Rd, Toronto, Ontario M4E 2L2 CANADA:

Microchess, A Chess Playing Program for the 6502 processor. Price: $13.

Microchess, A Chess Playing Program for the 8080 processor. Price: $18.

Circle 48 on inquiry card.

KIMSI

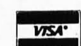


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Take a Course in Microprogramming

Richard Mac Millan
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As is becoming the case for more and more people, my job is bringing me into contact with the quickly evolving field of microprocessors and their applications. This I find fortunate because for several years I have had an intense interest in these gadgets and their potential use in certain hobbyist applications.

My employer and I agreed that it would be useful for me to learn as much as possible about microcomputers in order to evaluate their future impact upon the transportation field. (I'm an engineer in automotive electronics.) To that end I started looking around for a seminar that I might attend.

One that caught my eye, a course given by Wintek Inc, offered a "free" microcomputer to each participant. The 3 day seminar that was being offered included a discussion of microcomputer hardware and software as well as hands on experience in a laboratory. The program was based on the 6800 processor family for illustrative and training purposes.

Having signed up for the Wintek course in advance, I presented myself at the appointed time and place (a meeting room at a local Sheraton Inn). The Wintek program was presented by Dr Paul Wintz and Jim Wilson, the founders of the company.

Of the 35 participants, most were either engineers who, like myself, wanted to broaden their knowledge of microcomputer programming, or they were professional programmers looking to increase their understanding of small systems applications. Several turned out to be computer hobbyists as well. Most seemed to be lured to this particular course by the offer of a free microcomputer.

Material for the course was organized into a large 3 ring binder which provides an excellent reference after the course is concluded. The first morning (Tuesday) we spent learning our way around the 6800 system. The bus structure was described in some detail as was the addressing of IO and memory. The 6800 instruction set was introduced as well as the various addressing modes that may be applied to each instruction.

Wintek has developed its own read only memory monitor program which it calls FANTOM II. FANTOM II is resident in a 1 K read only memory on the 1 card computer Wintek gives its students, and is socketed so that it can be replaced with either a 2704 or a 2708 if desired.

FANTOM's use was reviewed before lunch on the first day. After lunch the class broke into two groups with one going into the first lab session and the other continuing in a lecture.

Lab consisted of a cluster of video terminals each connected to a Wintek 1 card microcomputer. Students worked in pairs on problems outlined in the course notes. An instructor was always available for assistance. The first afternoon in the lab was spent using the monitor program to load a simple routine into the computer and then debug it.

At coffee break, the two groups switched: students coming out of the lecture took a turn at the lab work. The rest of the course was spent alternately in the lab and in the class.

The Wednesday lecture discussed the various types of memories, their applications and trends to look for in the future. The IO devices of the 6800 family were also covered. The 6850 serial IO port (really an intelligent UART style interface device) was presented both as hardware and in terms of its use when programming to communicate with external equipment. The 6820 was then discussed. This device is a dual programmable 8 bit parallel IO port. Both the serial device and the parallel device interface directly with the 6800. Finally, time was spent learning the various ways that interrupts can be handled.

One of the best features of this course was the lab work. Working from simple programs to ones of more complexity with the aid of an instructor helps to build confidence in oneself. My lab partner and I worked our way through a program that generated a time delay via a count down loop, then used the loop as a basis for a timekeeping function. The terminal's bell function was used to mark the seconds and then the whole thing was integrated into a program that performed a digital clock function.

By the time Thursday rolled around we were trying to service interrupts from the video terminal in the middle of the timekeeping program. For those with more proficiency at machine language programming, there were more challenging projects, including a program to decode Morse code.

Lecture for Thursday turned to a comparison of the various microprocessor

families currently available. The advantages and drawbacks of each were compared. The area of applications that each is best suited for was discussed. Software aids to programming such as assemblers, editors, debuggers and compilers were explained and their operations were illustrated.

While understandably Wintek's products and services were mentioned at appropriate places throughout the course, no real hard sell was used. Their products were used primarily as an illustration of what is available to the user and as such was a useful part of the curriculum.

The Wintek computer given to each course participant consists of a 6800 processor, a 6820 peripheral interface adapter (PIA), a 6850 asynchronous communications interface adapter (ACIA) (serial IO for communication with a Teletype or RS-232 compatible terminal), two 6810 128 by 8 random access memory chips, a 1 K read only memory containing Wintek's FANTOM II monitor, a 600 kHz clock and a bps rate generator. Providing power (5 V, 12 V, -12 V), a reset button and a terminal is all that is required to be up and running.

Extra memory is available from Wintek but it is dynamic, requiring an extra card just for the refresh circuitry. The hobbyist would probably want to use a handful of 2102s instead. Provision is made on the Wintek card for two more memory chips, bringing the total read/write memory to 512 by 8.

I mentioned at the beginning that several of us in the class happened to be hobbyists. By the time we all had had a chance to actually work on the computers, most of us who were at first uncommitted became converts. We left clutching our microcomputers with thoughts of borrowing a terminal and writing our own programs.

Now, most hobbyists would hesitate to spend $500 of their own funds to attend a course like this. That much money would buy a lot of goodies or even a basic home system. Happily, many employers are willing to invest in such a program where there is a likelihood that the participant will bring state of the art knowledge and very useful experience back to work.

People who, like myself, are looking for a generalized survey of the current state of the art, in addition to some actual programming experience, might do well to seek a group such as Wintek in order to take a course. While I may not have finished the course an expert microprogrammer, I certainly have learned the basics necessary to know where to start on nearly any microprocessor project.■

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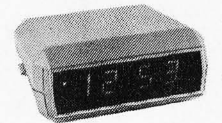
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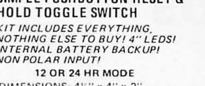
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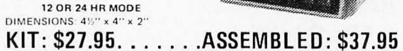


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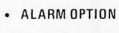
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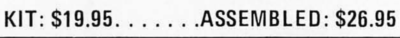
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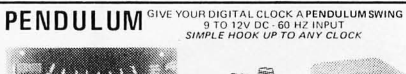


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This article demonstrates how software can be written to allow your computer to be used as an educational device. Having just gone through the exercise of helping my children learn all the states and their capi-

```
1 PRINT CHR$(26):PRINT CHR$(7):PRINT CHR$(7)
5 CLEAR 1000
10 DIM A$(50), B$(50)
20 FOR I=0 TO 49
30 READ A$(I), B$(I)
40 NEXT
50 PRINT "THIS PROGRAM WILL TEST YOUR KNOWLEDGE OF THE STATES AND"
60 PRINT "CAPITALS. AFTER EACH STATE (SELECTED AT RANDOM) PLEASE TYPE"
70 PRINT "IN THE APPROPRIATE CAPITAL FOLLOWED BY A 'RETURN' "
80 PRINT:PRINT
90 N=0:C=0:W=0
100 N=N+1: IF N>10 THEN 400
105 I=49*RND(-1)
106 I=INT(I)
108 Q=0
110 PRINT "WHAT IS THE CAPITAL OF ";A$(I);:INPUT Z$
120 IF Z$=B$(I) THEN 200
130 PRINT "NOT CORRECT!. . .TRY AGAIN":W=W+1
140 Q=Q+1:IF Q>=2 THEN 800
150 GOTO 110
200 R=4*RND(-1)+1:C=C+1
201 R=INT(R)
210 IF R=1 THEN 300
220 IF R=2 THEN 301
230 IF R=3 THEN 302
240 IF R=4 THEN 303
250 PRINT "CORRECT. .YOU'RE A GENIUS!!":GOTO 100
300 PRINT "CORRECT. .YOU'RE EXCEPTIONAL!!":GOTO 100
301 PRINT "CORRECT. .AMAZING ABILITY!!!":GOTO 100
302 PRINT "CORRECT. .YOU'RE TOO MUCH!":GOTO 100
303 PRINT "RIGHT ON!. .CARRY ON!":GOTO 100
400 PRINT "YOUR SCORE IS";C;"CORRECT";W;"WRONG";"RATING";C/(C+W)*100;
401 PRINT "%"
402 PRINT "DO YOU WISH TO CONTINUE THE LESSON (TYPE YES OR NO)?"
403 INPUT C$
404 IF C$ = "YES" THEN 90
405 IF C$ = "NO" THEN 830
406 GOTO 402
600 DATA MASS.,BOSTON,MAINE,AUGUSTA,VERMONT,MONTPELIER
610 DATA NEVADA,CARSON CITY,NEW HAMPSHIRE,CONCORD,NEW YORK,ALBANY
620 DATA NEW JERSEY,TRENTON,CONN.,HARTFORD,VIRGINIA,RICHMOND
630 DATA W.VIRGINIA,CHARLESTON,MARYLAND,ANNAPOLIS,N.CAROLINA,RALEIGH
640 DATA S.CAROLINA,COLUMBIA,FLORIDA,TALLAHASSEE,GEORGIA,ATLANTA
650 DATA ALABAMA,MONTGOMERY,ARKANSAS,LITTLE ROCK,MISS.,JACKSON
660 DATA WASHINGTON,OLYMPIA,N.MEXICO,SANTA FE,N.DAKOTA,BISMARCK
670 DATA S.DAKOTA,PIERRE,IDAHO,BOISE,ILLINOIS,SPRINGFIELD
680 DATA OHIO,COLUMBUS,INDIANA,INDIANAPOLIS,IOWA,DES MOINES
690 DATA KANSAS,TOPEKA,MISSOURI,JEFFERSON CITY,OKLAHOMA
700 DATA OKLAHOMA CITY,COLORADO,DENVER,UTAH,SALT LAKE CITY
710 DATA HAWAII,HONOLULU,ALASKA,JUNEAU,TEXAS,AUSTIN,LOUISIANA
720 DATA BATON ROUGE,PENN.,HARRISBURG,RHODE ISLAND,PROVIDENCE
730 DATA WISCONSIN,MADISON,MINN.(ABBREV.),ST. PAUL,MICHIGAN,LANSING
740 DATA KENTUCKY,FRANKFORT,TENNESSEE,NASHVILLE,NEBRASKA,LINCOLN
750 DATA MONTANA,HELENA,WYOMING,CHEYENNE
760 DATA DELAWARE,DOVER
770 DATA CALIFORNIA,SACRAMENTO,OREGON,SALEM
780 DATA ARIZONA,PHOENIX
800 PRINT:PRINT:PRINT "WELL, I GUESS YOU REALLY DON'T KNOW IT!! (SHAME)"
810 PRINT "THE CORRECT ANSWER IS ' ";B$(I);" ' NOW I WILL ASK YOU AGAIN.!"
820 GOTO 108
830 END
```


Circle 111 on inquiry card.

tals, it occurred to me that this might be readily automated using a computer and BASIC.

The program in the listing is written to run in MITS 8 K BASIC in about 3 K bytes of memory. It easily fits into my Altair system which has 12 K bytes of memory.

All the states and their capitals are listed in the DATA statements beginning on line 600. The arrays A$ (I) and B$ (I) are initialized with the BASIC READ statement embedded in a FOR. . .NEXT loop at lines 20 to 40. As you can see by the logic, each state and its corresponding capital are listed as a pair of strings in the DATA statements. As the variable I goes from 0 to 49 the first state name will be in A$ (0) and the capital of the first state will go into B$ (0); the n^{th} state name will go into A$ (n) and the n^{th} state capital will go into B$ (n).

In operation, the program is a loop which keeps generating random state selections and quizzing the student. A number I between 0 and 49 is chosen at random in line 105 using the RND function, which returns a value from 0 to 1. The corresponding state A$ (I) is selected and the question is generated. The student answers with an input which is stored in Z$. If the input from the student in Z$ is equal to the capital B$ (I) of the selected state the program will execute the "reward" subroutines. If the answer is not correct, then the question is repeated one time. If the correct answer is not given the second time, the computer then provides the correct answer and repeats the question in order to aid in the learning process. If the correct answer is given, the student is rewarded with a positive response, such as "Right on; carry on" or "You're exceptional." This response is also selected using a random number generator in order to provide a bit of variability in the reward statement. After ten states and capitals are provided, the computer gives a score summary with a percent evaluation of the student's responses.

The above programming concept can be applied to almost any teaching situation where an answer word or phrase can be directly associated with a question. The questions and answers are conveniently stored in the data lines within the program and are separated only by commas.

We have had fun making up this program and managed to learn a few of the states and their capitals in spite of it all!■

Circle 8 on inquiry card.

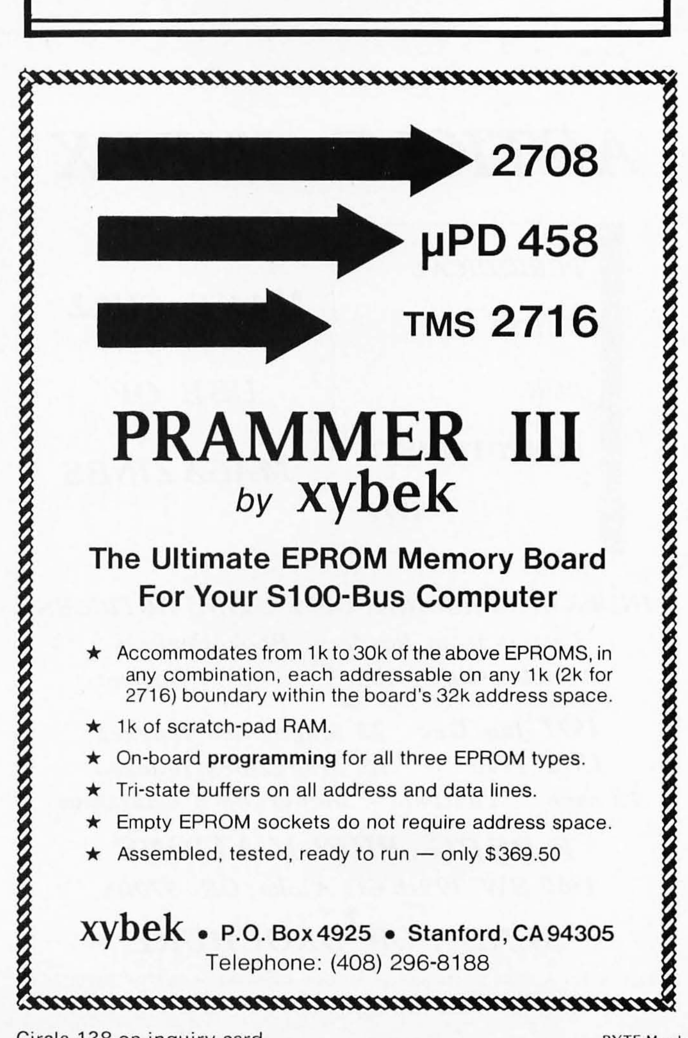
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Clubs and Newsletters

Conducted by
David Wozmak

Philadelphia Area Computer Society

The Philadelphia Area Computer Society was formed to educate computer users in the Philadelphia area and to inform the general public about computer technology and its implications for the future. Membership is open to all persons interested in any aspects of the computer arts and sciences.

Dues are $10 for regular membership and $5 for students. Both include a subscription to *The Data Bus* as well as participation in group purchase programs and club projects. Members also receive borrowing privileges in the Society's software and literature library.

PACS meetings are held in the LaSalle College Science Building at the corner of 20th and Olney (12 blocks north of US 1 on Broad St). Write to PACS, POB 1954, Philadelphia PA 19105.

NCCS

The Northwest Computer Society meets at the Pacific Science Center in Seattle on the first and third Wednesday of each month at 7:30 PM. The first meeting of the month is usually formal, involving a featured speaker or a demonstration. The second meeting of the month is usually more informal, with discussion and problem solving. The group also publishes a newsletter, *Northwest Computer Club News.*

Call Roy Gillette at 524-0596 (evenings) for more information, or write Northwest Computer Club, POB 242, Renton WA 98055.

The New York Amateur Computer Club

The New York Amateur Computer Club is a group of people with varying backgrounds, abilities, and interests whose common goal is "to promote the free exchange of information about computers for personal use, and to encourage fellowship among those interested in computing."

Club dues are $10 annually, from July 1 thru June 30, or $5 if you join after January 1. Prospective members are sent one or two issues of *The Newsletter* free of charge and are encouraged to attend club meetings as guests. For more information, contact The New York Amateur Computer Club, Church St Station, POB 106, New York NY 10007.

Association of Computer Experimenters

This group, located in Hamilton, Ontario, puts together a huge newsletter, *IPSO FACTO,* which has all kinds of information. The last issue I saw had several articles on cassette interfacing, including the Kansas City Standard, Data Formatting, etc. For more information, contact Tom Crawford at 50 Brentwood Dr, Stoney Creek, Ontario CANADA L8G 2W8.

Central Florida Computer Club

The Central Florida Computer Club has been in existence for over a year and has over 50 members. You can contact them by writing to John W Neel, 2821 Sunset Rd, Apopka FL 32703.

NCCCCC (NC[5])

On May 5 and 6 the Northern California Community College Computing Consortium (whew) Spring Conference will be held at Sierra College, 5000 Rocklin Rd, Rocklin

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CA 75677. Contact Perry Edwards at (916) 624-3333 for details, or write to him at the above address.

65 Notes

65 Notes is the monthly publication of the HP-65 users club. It contains mainly programming twists and information concerning the HP-65. Also included are programs and club information. Contact Richard J Nelson, 2541 W Camden Pl, Santa Ana CA 92704.

San Diego Computer Society

This group publishes a well put together newsletter, *Personal Systems.* It contains club information, programs and so on.

The San Diego based club has special interest groups on the Z-80, 6800 and 1802, 6502, 8080, as well as groups on biofeedback, education, graphics, and word processing in the legal profession. The address is San Diego Computer Society, POB 9988, San Diego CA 92109.

The Computerist

This newsletter, edited by Mark Browne and Geoff Wattles, covers four different clubs: The Minnesota Computer Society (MCS); Small Computer Engineering Association of Minnesota (SCEAM); University Microcomputer Group (UMG); and Advanced Technology Research Association (ATRA).

The newsletter contains information concerning all the clubs, including meeting dates. The March dates are as follows: SCEAM: March 30; UMG: March 1, 8, 15, and 22; MCS: March 5; ATRA: March 7, 14, 21, 28.

For more information concerning the clubs, write to Mark Browne, 3504 Stevens Av S, Minneapolis MN 55408.

Homebrew Computer Club

The Homebrew Computer Club meets regularly at the Stanford Linear Accelerator Center Auditorium (SLAC). During the past two years, attendance has increased from thirty people to over two hundred. The Homebrew Computer Club, which also publishes a newsletter, can be reached at POB 626, Mountainview CA 94042.

West Virginia Computer Society

Oscillations is the name of the West Virginia Computer Society's newsletter, which features short articles about new microprocessor developments, video games, local computer news, and so on. For information on the time and location of local meetings, contact Bill England at WVCS, 167 Iroquois Trail, Ona WV 25545. ■

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The Relocating Assembler and the Linking Loader are furnished on cassette in relocatable formatted code, so they may be placed anywhere in memory. A short mini-loader program in standard Mikbug format is supplied to initially load the Linking Loader at any desired address. A comprehensive Instruction Manual and an extensively commented assembly listing complete the M68AS assembler package.

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M6800 Source Generator	M68SG	25.00
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For many experimenters, the microprocessor is an excellent source of mind stimulation, and that is a laudable end in itself. But after you figure out how a computer works, perhaps build one, and play various games with it, you might want to try your hand at process control.

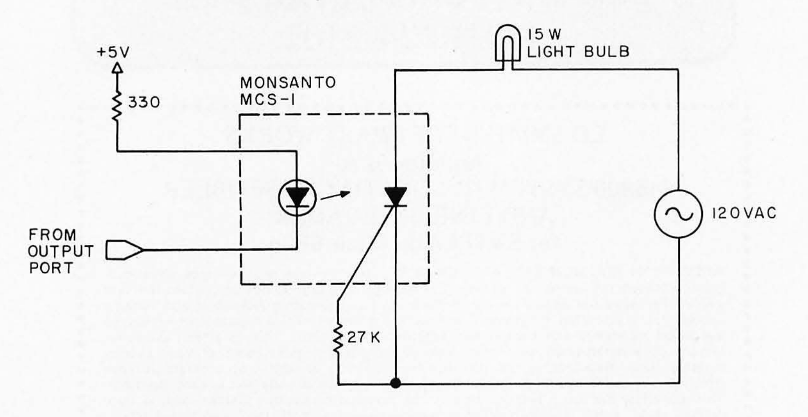


Figure 1: Simple half wave control of AC operated devices using an SCR (silicon controlled rectifier) optocoupler.

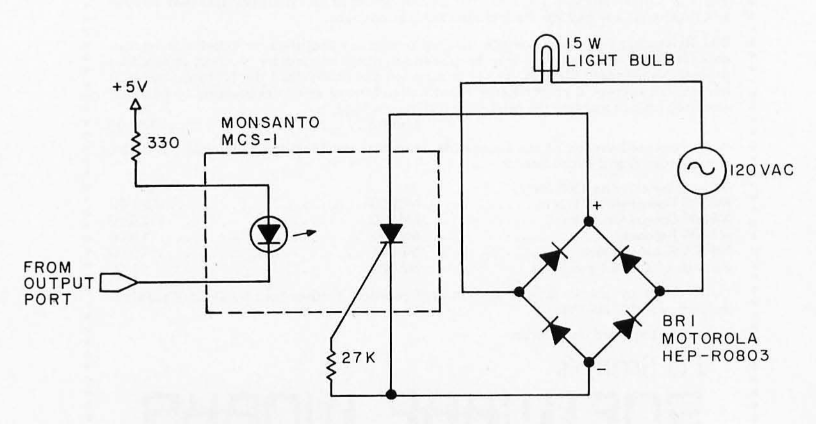


Figure 2: Full wave control of AC operated devices using an SCR optocoupler.

Industry looks upon the microprocessor as the controller of processes, whether as large as a steel rolling mill or as small as a telephone instrument. And, indeed, the microprocessor may be one way to help solve the automobile emission problem, the fuel crisis in home heating, and a myriad of other current social problems.

The output of an appropriate set of ones and zeros by the microcomputer (after it has digested all its inputs and instructions) is all that is required to solve the problem, theoretically. However, there still remains a fair gap between the microcomputer output and the closure of a solenoid valve in a piece of machinery, for instance.

Figure 1 shows one such real world application, an SCR (silicon controlled rectifier) optocoupler used to control a 117 VAC line operated device with microcomputer output logic voltages. This circuit will certainly work, but the light bulb load will light only to half brilliance because the SCR conducts only on the positive half cycle of the AC line voltage. One way of getting around this is to modify the circuit, as shown in figure 2, by using a diode bridge in conjunction with the SCR photocoupler. This is an old trick developed to allow SCRs to be used for full-wave control. It came into use before the introduction of the Triac.

There is another way of achieving full wave AC control: Use a dual SCR optocoupler such as the Monsanto MCS6200. Since there are two light emitting diodes and two photo-SCRs (each LED controls its own photo SCR), one can connect the LEDs in series and the photo SCRs in reverse parallel to create the equivalent of a Triac photocoupler. This connection is shown in figure 3. (The MCS6200 is useful for other applications, of course, such as polarity reversal.)

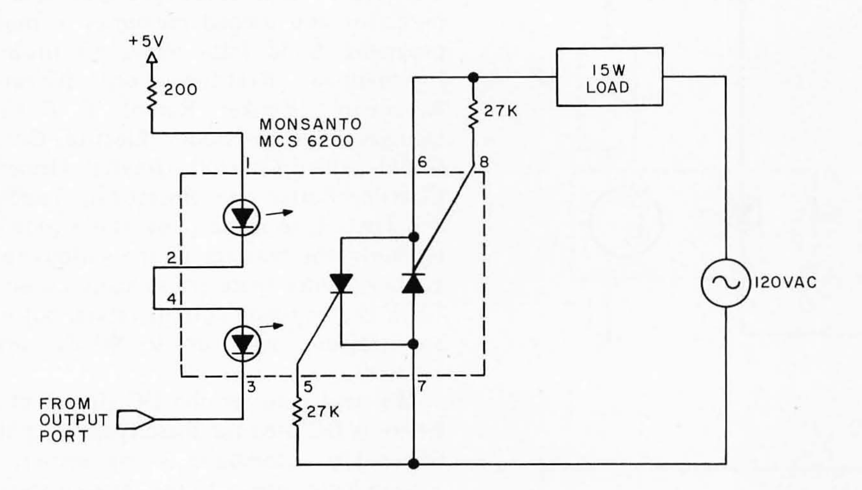


Figure 3: Using a dual SCR optoisolator for full wave control of an AC operated device.

The MCS-1 and MCS6200 are rather limited in their current handling capability, however. The MCS-1 will carry 250 mA and the MCS6200 will carry only 150 mA. This sort of capability is fine for lighting small light bulbs, but hardly suitable for the types of loads found in real process controls.

When working with 117 VAC control schemes, zero voltage turn on and zero current turn off are desirable design goals. If we had a logic controlled device capable of closing the AC connections only when the AC voltage is crossing through zero, a number of problems would be solved. (AC voltage alternates sinusoidally, crossing the zero voltage point twice per cycle.) The large inrush current that can occur when an AC switch is closed at (or near) the positive or negative peak of the AC sine wave can be eliminated by such a zero voltage turn on device. Zero current turn off techniques have the added advantage of not interrupting large currents in mid flow. If the AC load is a pure resistance such as a light bulb or heater, the zero voltage and zero current points are coincident in time; but, in general, AC loads will have inductive or capacitive reactance. The current and voltage waveforms will therefore be not quite in phase. For general use, we wish our logic controlled AC switch to have both zero voltage turn on *and* zero current turn off. Such a device is the modern solid state relay.

The Monsanto MSR100B is a good example of the solid state relay. As with other optically coupled devices, the solid state relay maintains complete isolation from the logic level controlling system. The MSR100B is shown in block diagram form in figure 4. The device is rated for 10 A at 120 VAC. So up to 1.2 kW can be controlled with only TTL level inputs. The modern solid state relay has a myriad of protective features built into it (see figure 4). The zero voltage turn on and zero current turn off features contribute most to the desirability of the solid state relay since they can attenuate line transients and radio frequency

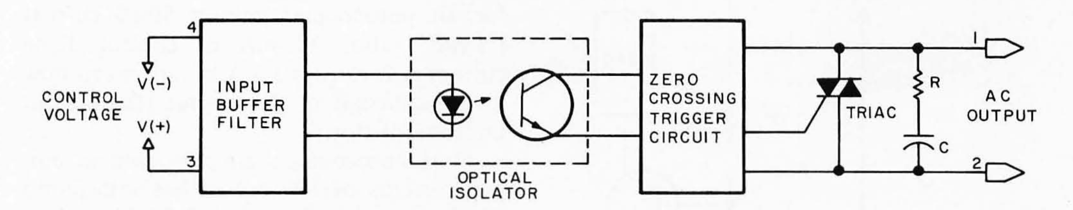


Figure 4: A typical solid state relay. Units such as this Monsanto MSR 100/200 have many convenient features. The zero voltage and zero current switching abilities eliminate damaging high current surges to the load, as well as high voltage transients experienced with inductive loads. The input filter prevents short duration noise (<10 µs) of signal strength from falsely switching the relay. The output filter suppresses transient signals generated either from inductive loads or long lines.

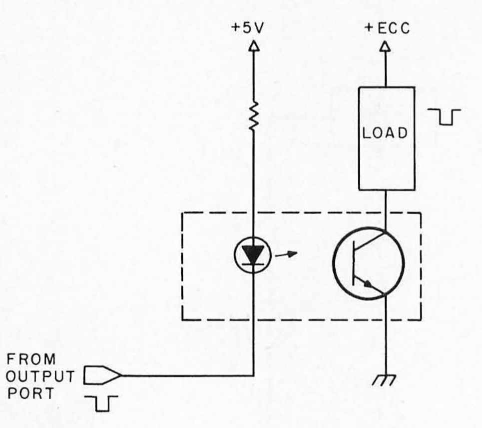


Figure 5: Use of an optocoupler to directly control a relatively small load.

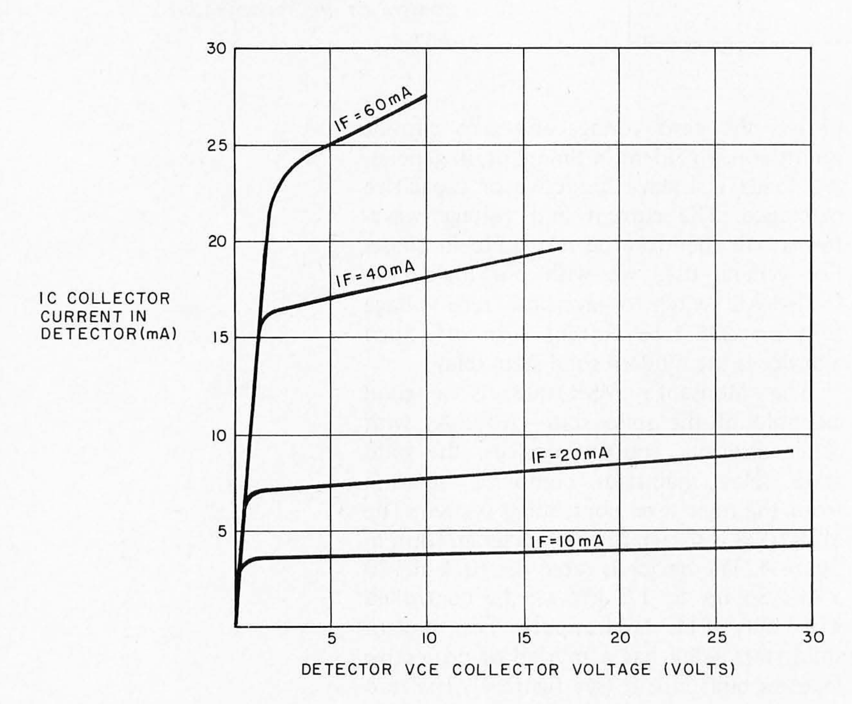


Figure 6: Monsanto MCT-1 solid state relay characteristics for various LED currents.

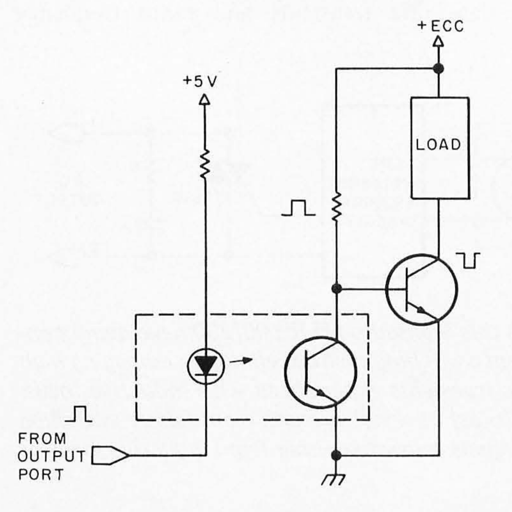


Figure 7: Use of an external NPN transistor to increase load current control capabilities.

interference that could get back into the processor and unload memories or modify programs. Solid state relays are made by International Rectifier Corp (Crydom), Amphenol (Runker Ramo), C P Clare, Douglas Randall (Kidde), Electrol, Gordos, Gould (Allied Control), Grayhill, Heineman Electric, Potter and Brumfield, Teledyne, and Theta-J, to name a few. It is a good idea to study the features of the various relays available, since there are so many variations. 10 A is a common current rating, but units are available with up to 40 A current capacity.

We next consider the DC side of things. Where is DC used for these types of applications? The automobile is one answer. The auto industry hopes to use microprocessors, but must operate them from +12 VDC for reasons of practicality. The SCR optocoupler in figure 1 can not be used for DC control, unless one wishes the DC being controlled to latch "on." That is, once the controlling diode turns the photo SCR "on" (with a DC supply of the proper polarity), the SCR will stay on no matter what the control current does. In order to control DC, it is a better plan to use a more conventional optocoupler, ie: one that has a phototransistor as the output device. Such optocouplers are widely available from most of the semiconductor producers. Among the producers of optocouplers are Fairchild, Hewlett-Packard, Litronix, Monsanto, Motorola, and Texas Instruments.

An example of the use of optocouplers for isolated DC control is shown in figure 5. A Monsanto MCT-1 is used in this circuit, which has a characteristic like that shown in figure 6. The MCT-1 is an early optocoupler, and it has a rather low ratio of collector output current to photo diode input current (about 35%). Newer optocouplers, using photo Darlington transistors, can have a ratio of 500% or more. That is, for an optocoupler with a 500% current transfer ratio, 10 mA of control diode current will cause 50 mA of current to flow in the collector of the output (Darlington) photo transistor.

Most optocouplers are restricted to output currents of 100 mA or less with photo transistor voltage ratings of 30 V or less. (There are exceptions, like the Monsanto MCA2200, which will stand 200 V.) A capability of 30 V and 100 mA means that optocouplers can handle relatively small loads of only a few watts. This is not a problem, since the optocoupler can be

followed by a power transistor whose current gain, voltage rating, and current rating can increase the capability to control hundreds of watts. Three ways that this can be done are shown in figures 7, 8 and 9. Note that using an external transistor to increase voltage or current capability may cause an inversion of the logic, but this can be easily corrected either in software or by the addition of a single 7405 inverter section on the logic side of the optocoupler.

Many devices used in process control have inductive reactance as part of their impedance. As a result, when switching relays, solenoids or motors with transistors (whether directly from the photo transistor of the optocoupler or by means of an external transistor) it is desirable to add "inductive kick" protection. The inductive kick occurs when the transistor attempts to turn off the inductive load. At this point, the collector voltage can easily exceed the maximum rating. A diode across the inductive load will protect the transistor as shown in figure 10.

Another method of protection is the use of a thyrite varistor as in figure 11. The thyrite varistor must be chosen so as to draw reasonable current when the normal coil voltage is present across it; thyrite varistors are nonlinear resistors and draw abnormally high current when the voltage across them increases (during the inductive kick).

For general reference on the subject of the various optically isolated couplers discussed here, references 3, 4, and 5 are recommended. The catalogs of such producers as Monsanto are also useful; brief application data often accompany the data sheets.■

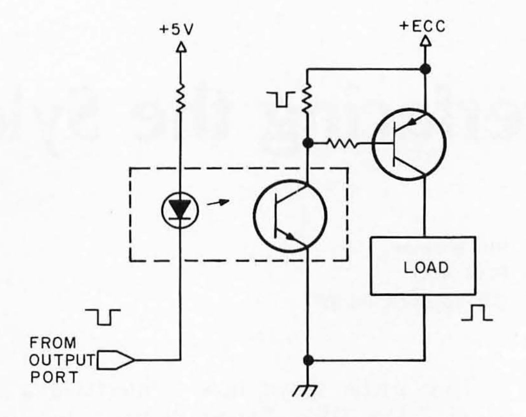


Figure 8: Using an external PNP transistor to increase the load current capability. This circuit is useful when the load must have one side common to the control system ground.

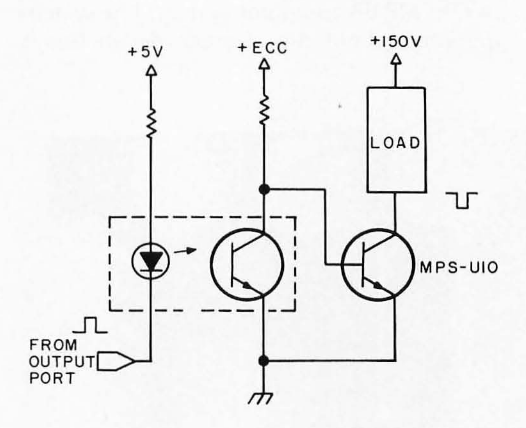


Figure 9: Use of a high voltage NPN transistor to drive a load requiring high DC voltages.

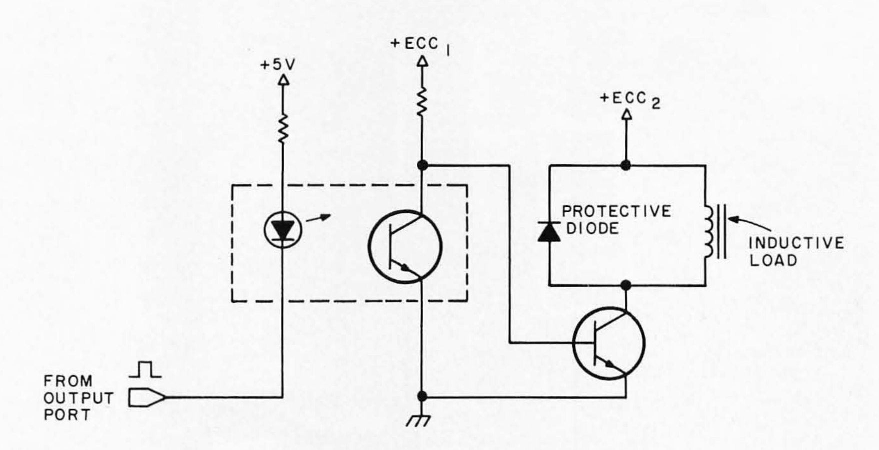


Figure 10: Using a diode to protect the drive transistor from an inductive kick voltage overload.

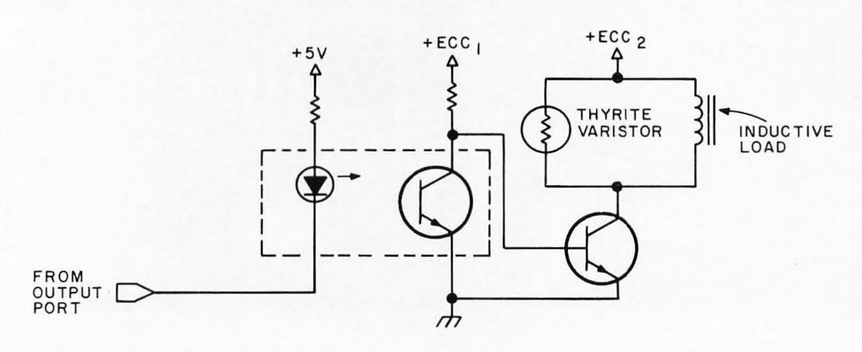


Figure 11: A circuit which uses a thyrite varistor to protect the driver transistor from an inductive kick voltage overload.

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1. General Electric, *Silicon Controlled Rectifier Hobby Manual*, 640.8, pages 31 thru 34, 1963.
2. Smith, G, "Applications of Opto-Isolators," *Lightronix Appnote 2*, Litronix Inc, 19000 Homestead Rd, Vallco Park, Cupertino CA 95014.
3. Hewlett-Packard, "Optoelectronic Applications Seminar (Notes)," 592-0343, Hewlett-Packard, 1501 Page Mill Rd, Palo Alto CA 94304, 1972/1973.
4. Christian, F, "Isolation Techniques Using Optical Couplers," *Motorola Application Note AN 571,* Motorola Semiconductor, POB 20912, Phoenix AZ 85036, April 1973.
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Interfacing the Sykes OEM Floppy

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This article shows how I interfaced a Sykes 7158 OEM floppy disk kit to a SwTPC MP-68 computer system. The system presented is not the ultimate design but it has been built and it operates properly. I consider it a good basis for the development of a disk operating system.

First, let's look at the Sykes kit. The 7158 kit consists of an Orbis disk drive and a controller designed and built by Sykes which employs a 6502 microprocessor. This is one of the smarter controllers. The interface consists of only an 8 bit bidirectional bus and five control lines for hardware requirements. Software commands such as track select, read sector X and reset are used. Additional commands such as step head in and step head out are available but are only used for diagnostic purposes. Cost of the 7158 kit is about $1300.

Alternatives to the 7158 kit are the 7258, 7358, and 7458 kits which are similar but include two, three or four disk drives. Notice that the controller can handle up to four disk drives. Another alternative is the 9158 and its multiple drive relatives 9258, 9358 and 9458. These units offer greater packing density and therefore greater storage capacity. The capacity of a 7000 series drive is 256,256 bytes and 630,784 bytes for the 9000 series. If you need the extra capacity a 9000 series kit may be a better choice. However, this is Sykes' own format and is not likely to be compatible with anything else. The 7000 series units are compatible with the IBM 3741 format.

If you are unfamiliar with the IBM floppy disk format it is composed of 77 tracks numbered 0 through 76. Each track is divided into 26 sectors numbered 1 thru 26. Each sector consists of four fields as shown in figure 1.

Power requirements for the disk and controller are shown in table 1. A commercial power supply can be purchased or you can build your own supply. Figure 2 is a schematic of a power supply which supplies the needed voltages, offers voltage adjustment on the +24 and +5 supplies and has both adjustable current limiting and overvoltage protection on the 5 V supply.

Once the power requirements are satisfied we can get to the interface. My design goal here was to build the complete interface on a circuit board which would fit into an IO slot on the MP-68. This feat is shown in photo 1. This interface was built on a Personal Computing Company board using quasi wire wrap techniques. This means that

Photo 1: The interface between the Southwest Technical Products 6800 system and the Sykes floppy disk subsystem was fabricated on this prototyping board for the SwTPC bus. The schematic is shown in figure 3.

Disk Kit to a Personal Computer

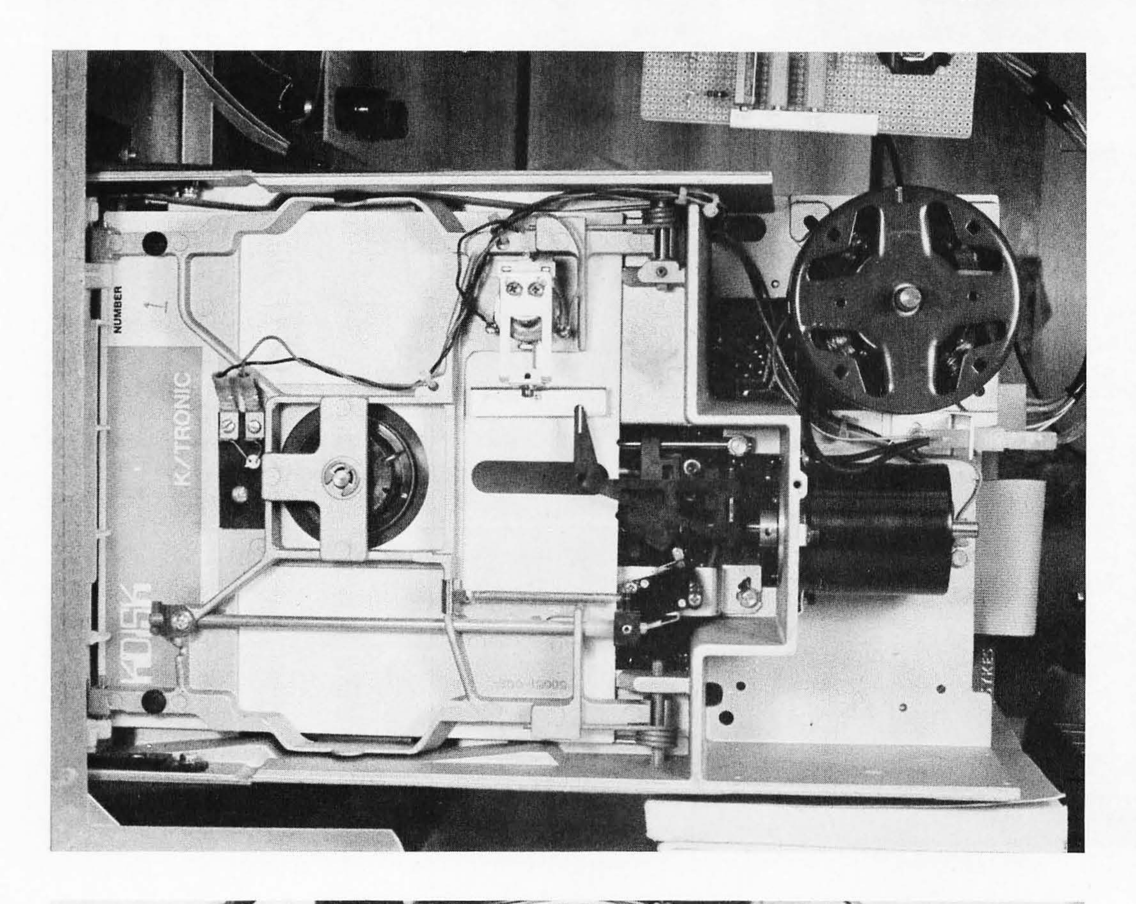


Photo 2a: Top view of the Orbis disk drive used by Sykes in its 7158 system, with the floppy disk inserted.

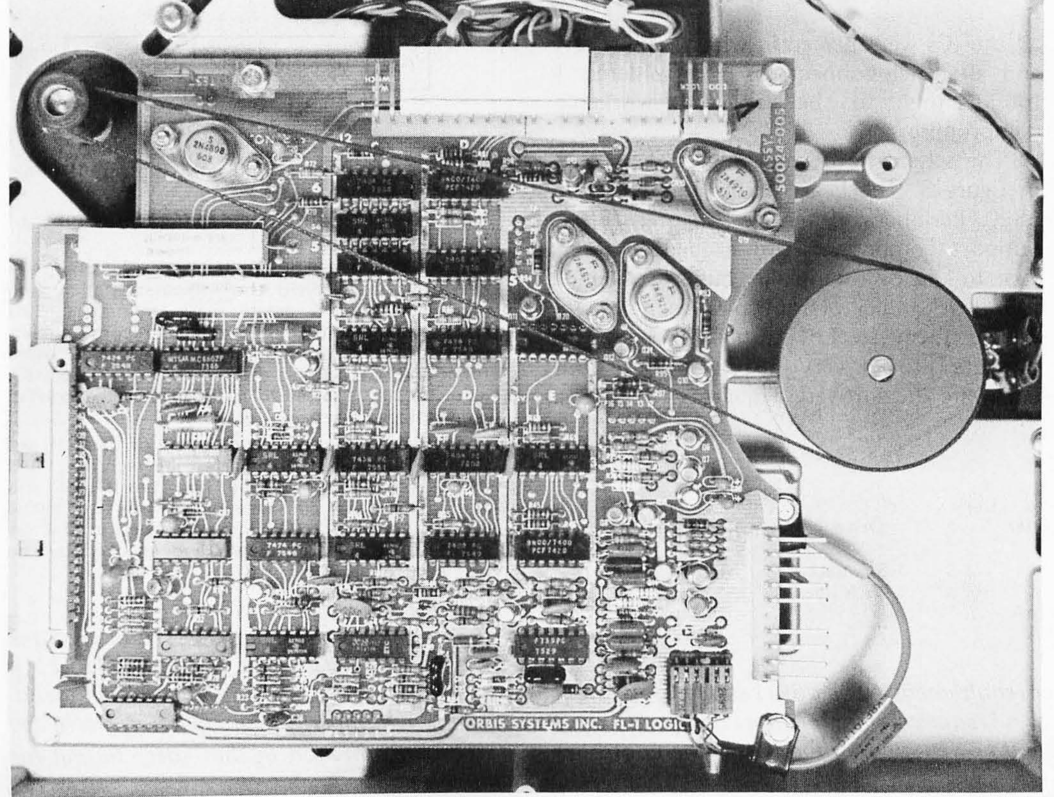


Photo 2b: Bottom view of the Orbis disk drive used by Sykes, showing the built in control electronics and belt drive for the disk spindle. The Sykes interface (photo 3) has been removed for this picture.

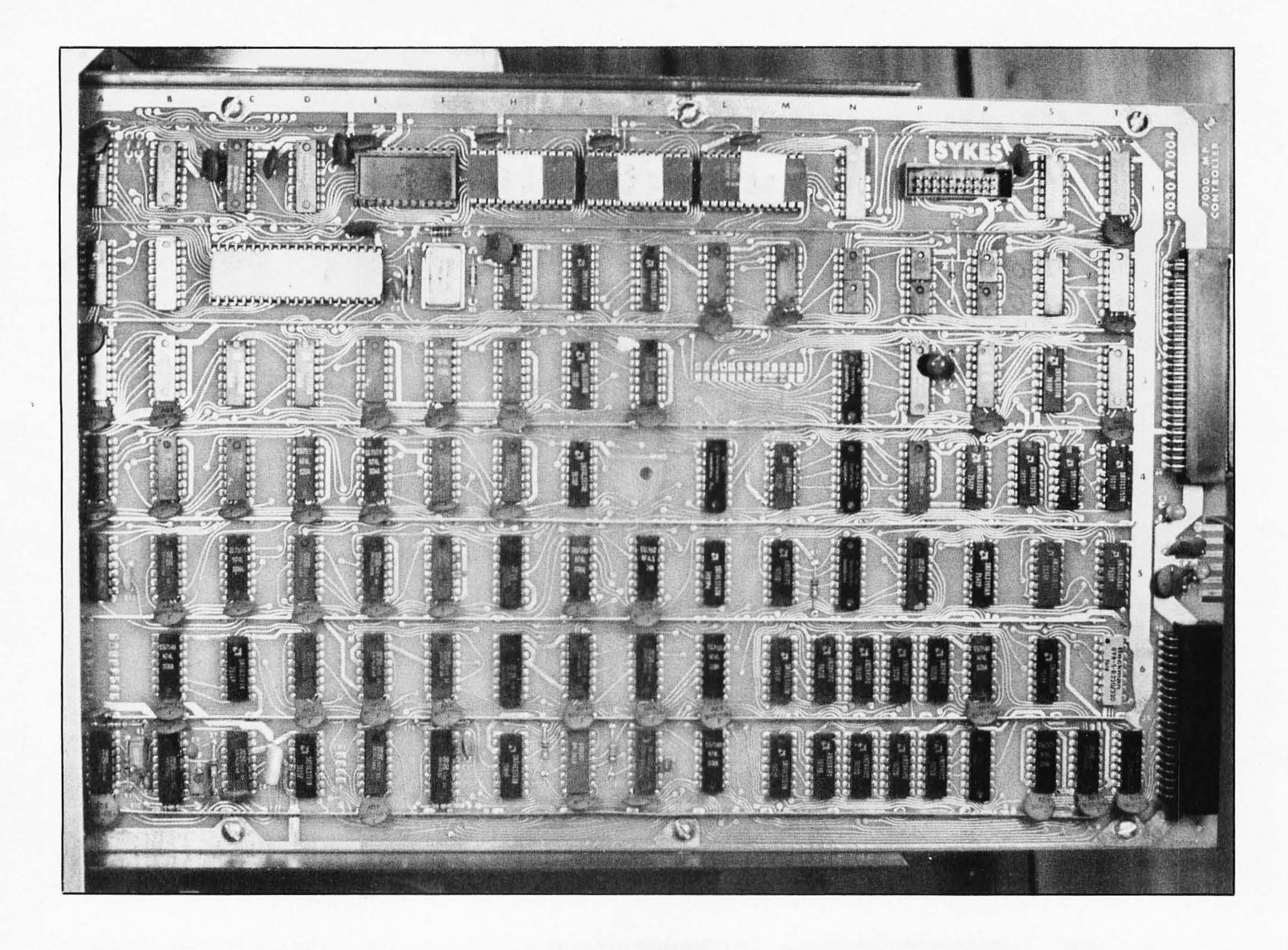


Photo 3: The Sykes floppy disk controller board. This board mounts on the bottom of the Orbis drive; it contains a 6502 processor with read only memory programming needed to implement the high level command sequences available on the bidirectional interface.

all the ICs were placed in wire wrap sockets and all other connections were soldered. I found this to be a very workable compromise.

The schematic of the interface is shown in figure 3. The heart of the interface is a 6820 Peripheral Interface Adapter (PIA). Support components are needed to interface to the disk controller bus. Also I built four level indicators and permanently connected them to TP1 thru TP4. These indicators proved very helpful during both hardware and software debugging.

Voltage	Controller	Drive	Total
+24 ± 10%		1.5 A max .75 A idle	1.5 A
−12 ± 10%	100 mA		100 mA
+5 ± 5%	3.0 A	.75 A	3.75 A

Table 1: Disk interface DC power requirements. The power supply of figure 2 was designed and built to meet these requirements; for those desiring to omit this detail, Sykes makes available a power supply module for the controller and drive.

AM	ID Field	DM	Data Field

AM = Address mark. Indicates that an ID field follows immedately.

ID Field = Identifies track and sector number of the following record.

DM = Data mark or delete mark. A data mark delimits the ID field and indicates that a good record follows. A delete mark delimits the ID field and indicates that a deleted record follows. Note that the deleted record flag is a software function. A read of a deleted record is processed; just the status is set to indicate that the deleted record flag was set.

Data Field = Contains 128 bytes of data. If less than 128 bytes are transferred the record is filled by the controller. Note that both the ID field and the data field are terminated by two cyclic redundancy check (CRC) bytes. These characters are automatically generated and checked by the disk controller.

Figure 1: Sector layout. The sector layout is fixed by the design of the controller. Each sector has 128 bytes of data, and an identification number which contains track and sector information in the "soft" format for floppies.

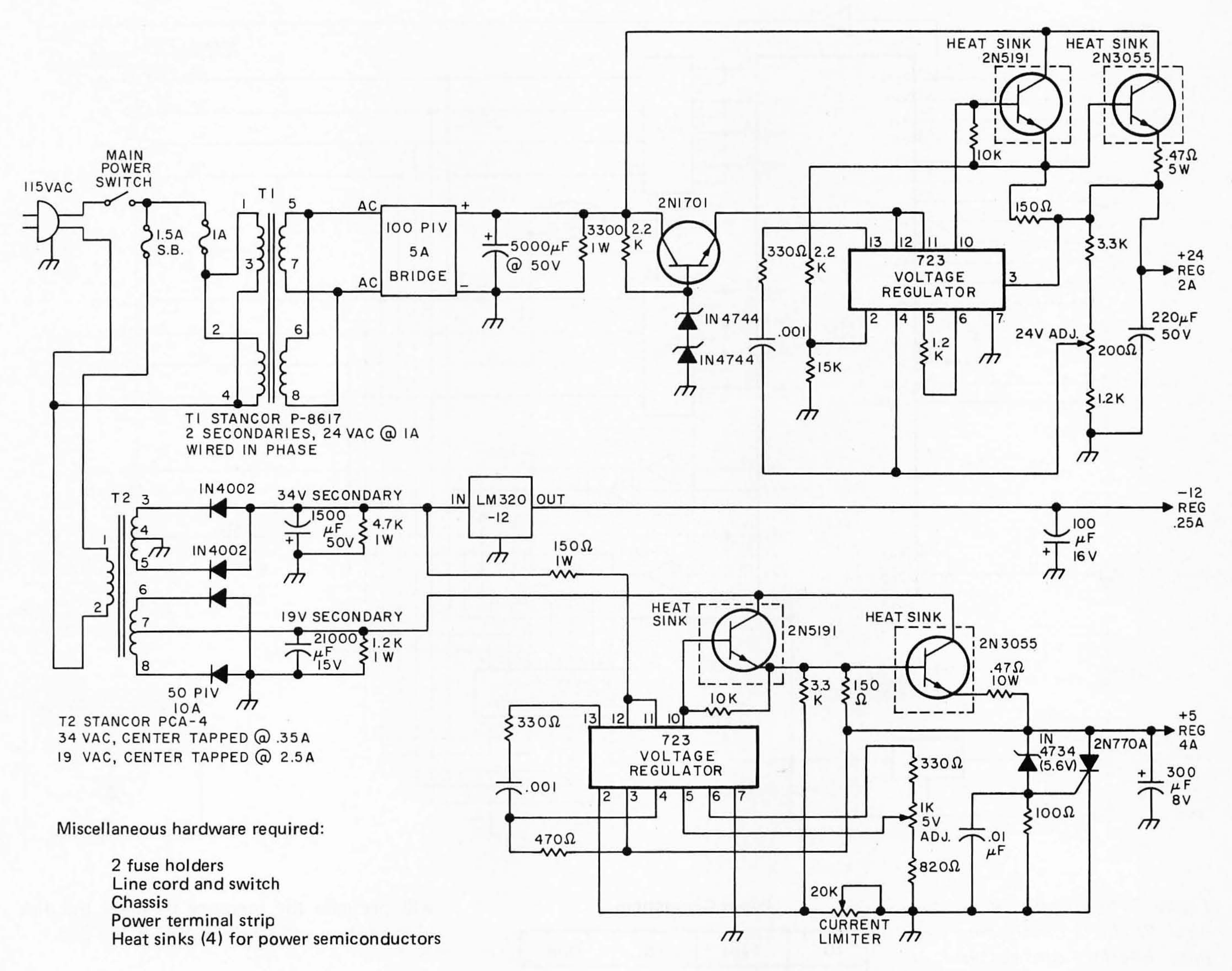


Figure 2: Power supply for disk system. This power supply uses the 723 voltage regulator IC to actively regulate a 24 V 2 A supply for the disk motor(s), and electronics supplies of −12 V at 0.35 A and 5 V at 4 A.

The software which I have developed is reasonably primitive but should be a valuable tool for use in the development of a disk operating system. It performs four functions. They are read (R), write (W), exit (X) and start (S). The read and write functions transfer the first 8 K bytes of memory to and from specified locations on the disk. The user is prompted for the location which is indicated by one character from A to P. This character is converted to a track address and the IO function is performed. After each operation the disk status byte is returned to the control terminal. The exit function returns control to the Motorola MIKBUG monitor. The start function performs a JMP to location 0100, the start address of the SwTPC software.

Condition	Hexadecimal Value of Bit	Bit Position
Deleted Record	80	Bit 7
Fault	40	Bit 6
Track 00	20	Bit 5
Disk Protect	10	Bit 4
CRC Error	08	Bit 3
Busy	04	Bit 2
Ready	02	Bit 1
Data Service	01	Bit 0

Table 2: Controller status byte. Each bit of this byte determines one flag signal sent back to the computer. Detailed information is included in the Users Manual For Series 7000/9000 OEM Systems Kit *which is supplied with the drive when it is purchased.*

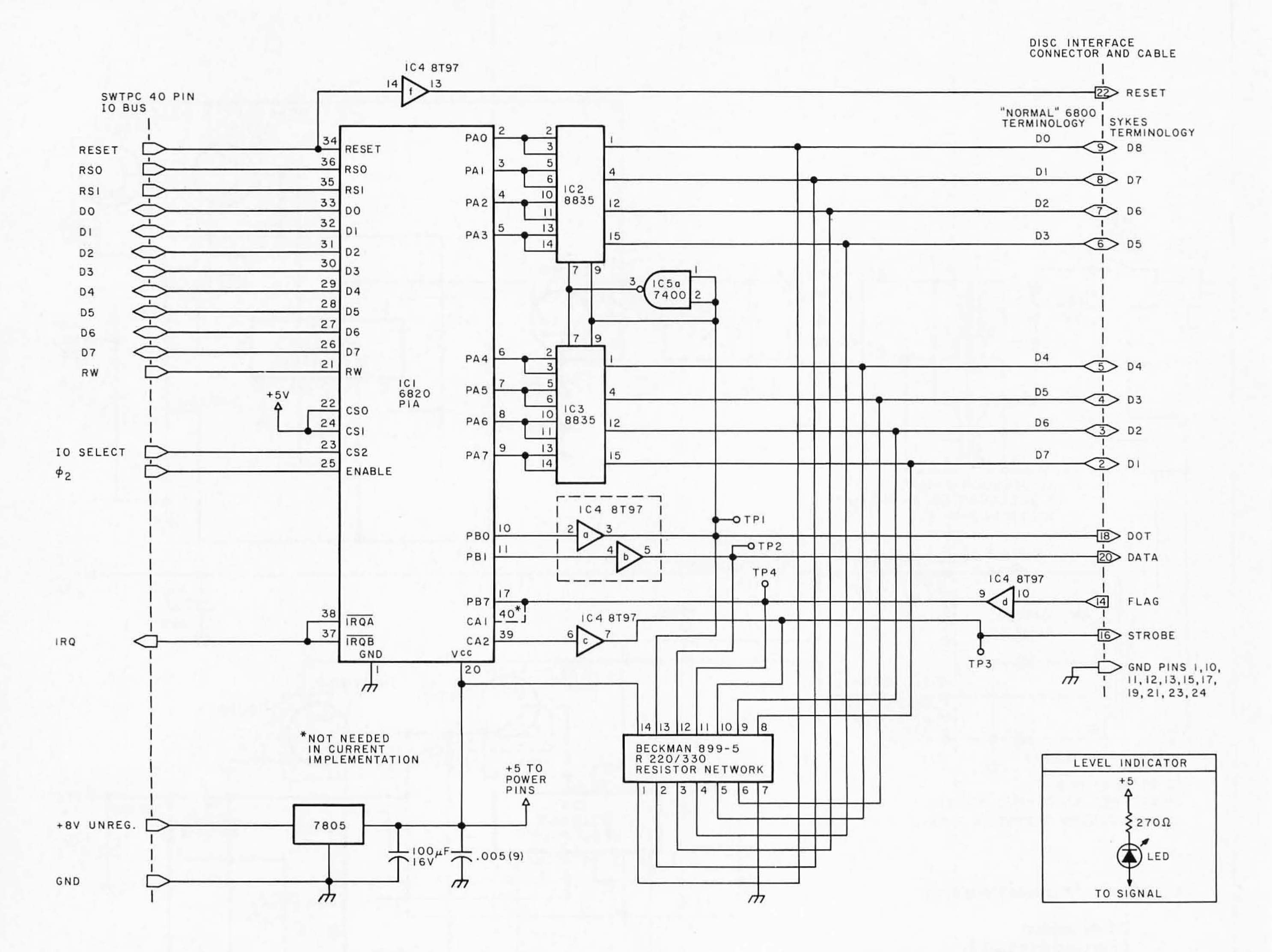


Figure 3: Southwest Technical Products 6800 computer interface card design for the Sykes floppy disk kit. A 6820 PIA part determines the state of the various interface lines and effects the transfers.

Power Connections

IC	Type	+5	Gnd
IC1	6820	20	1
IC2	8835	16	1
IC3	8835	16	8
IC4	8T97	16	1,8,15
IC5	7400	14	7

Using these basic functions, programs such as the Editor, Assembler, and BASIC can be loaded into memory and written out to disk so that they can be subsequently loaded from disk. The advantage: It takes about 30 seconds to load the disk load routine from cassette at 30 cps and then disk IO is performed at about 10,000 bytes per second. If you modify the Editor, Assembler, and BASIC so that they do not use the memory where DISKLD is located you will be able to load each program directly from disk.

For example, the following sequence can be used to modify 8 K BASIC so that it will preserve the memory used by the disk load routine and save 8 K BASIC on disk.

- Load 8 K BASIC from cassette or paper tape.
- Change memory location 0044-0045 to hexadecimal 2DFF. This is the upper memory limit that BASIC will attempt to use.
- Load DISKLD from cassette or paper tape and start.
- DISKLD should respond with "22LDR>." The 22 is the status as defined in table 2. If the status is other than 22 or 02 you should look it up in table 2 and determine what the problem is.
- In response to "LDR>" enter "W" (for write).
- In response to "ID–" enter the ID you wish to save BASIC under. (B is a logical choice.)
- DISKLD should respond with the status again (which should be 02) followed by another status and the "LDR>" message.

If the status is correct from the previous sequence you should now be able to load BASIC from the disk and start its execution by the following sequence.

- If the system has been powered down or DISKLD is not loaded, load it from tape and start.
- If the status is correct enter "R" for read.
- In response to "ID—" enter the ID of BASIC ("B").
- If the status is correct enter "S" to start execution.

For those who wish to dig in and start writing some fancy software DISKLD contains the following functional units.

- **DCNTRL** — Calls the PIA initialization routine, prompts the user for the desired function (R, W, X or S) and transfers control to the requested routine.
- **DINIT** — Sets up the PIA.
- **DCOMM** — Issues the command in the A accumulator to the disk and returns disk status in the A accumulator and PIA address in the index register (X).
- **DIPLR** — Prompts for ID and performs an 8 K byte disk read.
- **DIPLW** — Prompts for ID and performs an 8 K byte disk write.
- **DTERM** — Issues a terminate command to the disk controller, returns the status to the control interface and returns control to DCNTRL. Used by DIPLR and DIPLW.
- **DISKLD**—Designed to work with MIKBUG and with the disk interface connected to IO slot 0. The EQUs at the beginning of the program set up this environment and can be changed to meet the requirements of different configurations.

The hardware interface requirements are defined in detail in the documentation supplied with the disk kit. These basics should make the SwTPC interface more understandable:

- **D1** to **D8** are eight bidirectional data lines. Their direction and contents are defined by the status of the **DOT** and **DATA** control lines. Note that Sykes defined the high order bit as **D1** and the low order bit as **D8**. (Motorola and SwTPC define D7 as the high order bit and D0 as the low order bit.)
- **RESET** is a bidirectional, ground asserted signal. The interface is designed so that only the processor can send a reset command to the disk controller.
- **FLAG** is a controller originated, ground asserted signal. This signal informs the computer that the disk controller requires service.
- **DATA** is a computer originated, ground asserted signal. When asserted, the data lines (**D1** thru **D8**) will contain a data byte. When not asserted, the data lines will contain either a command (from the computer) or a status (from the disk controller).
- **DOT** is a computer originated, ground asserted signal. When asserted it indicates that the direction of transfer on the data lines is from the computer to the disk.
- **STROBE** is a computer generated, ground asserted signal indicating that information is being transferred on the data lines.

Section A of the PIA is used to handle the data lines. The peripheral control line CA2 is used to supply strobe information. The two low order bits of section B of the PIA are used to control the **DOT** and **DATA** control lines. Bit 7 of the B section of the PIA is used to receive flag information from the disk controller. Initially CA1 (PIA section A interrupt input) was to be used for the flag function; however, the current design of the DISKLD program can loose a flag status change. Using PB7 has proved to be easier to handle.

For those who wish to develop a disk operating system from the basic hardware and software I have the following suggestions. The easiest type of disk allocation system to handle and integrate into

Listing 1: Software of the primitive disk interface software used to test out the drive and provide a minimum level of mass storage function. DSKLD performs four functions:

R = read a block from disk.
W = write a block to disk.
X = exit the DSKLD program.
S = start a program at the assumed entry point of hexadecimal 100.

This program was assembled and listed using a printer with narrow width, so comments are somewhat restricted. The terminal command interpretation is done by means of a sequence of comparisons at addresses 2E14 to 2E22.

```
                      NAM    DISKLD
                      OPT    O
                      OPT    NOP
                      OPT    S
                      OPT    NOG
               *  SUPER SIMPLE DISK BOOT
               *
     E0E3      MIKBUG EQU    $E0E3
     E07E      PDATA1 EQU    $E07E
     E1AC      INEEE  EQU    $E1AC
     E1D1      OUTEEE EQU    $E1D1
     E0BF      OUT2H  EQU    $E0BF
     8000      DPIA   EQU    $8000
               *
2E00                  ORG    $2E00
     2E00      DCNTRL EQU    *
2E00 BD 2E38          JSR    DINIT
2E03 86 80            LDA A  #$80      RESE
T

2E05 BD 2E47          JSR    DCOMM
2E08 BD E0BF          JSR    OUT2H     PRIN
T STATUS

2E0B CE 2E33          LDX    #DCMSG
2E0E BD E07E          JSR    PDATA1
2E11 BD E1AC          JSR    INEEE
2E14 81 52            CMP A  #'R
2E16 27 12            BEQ    DCREAD
2E18 81 57            CMP A  #'W
2E1A 27 11            BEQ    DCWRIT
2E1C 81 58            CMP A  #'X
2E1E 27 10            BEQ    DCEXIT
2E20 81 53            CMP A  #'S
2E22 27 03            BEQ    DCSTRT
2E24 7E 2E00          JMP    DCNTRL
               *
2E27 7E 0100 DCSTRT JMP      $100
2E2A 7E 2E6B DCREAD JMP      DIPLR
2E2D 7E 2EA4 DCWRIT JMP      DIPLW
2E30 7E E0E3 DCEXIT JMP      MIKBUG
2E33 4C      DCMSG  FCC      /LDR>/
2E37 04             FCB      $04
               *
               * SUBROUTINES
     2E38      DINIT  EQU    *         INIT
IALIZATION

2E38 CE 8000          LDX    #DPIA
2E3B 6F 03            CLR    3,X       SELE
CT DD REG

2E3D 86 03            LDA A  #$3       SET
CONTROL LINES TO OUTPUT
2E3F A7 02            STA A  2,X
2E41 86 04            LDA A  #$04
2E43 A7 03            STA A  3,X       SELE
CT DATA REG

2E45 20 15            BRA    DSTAT
               *
     2E47      DCOMM  EQU    *         COMM
AND ISSUE

               *  INPUT:  A=COMMAND
               * OUTPUT:  A=STATUS
               *        : X=PIA ADDRESS
2E47 CE 8000          LDX    #DPIA
2E4A C6 02            LDA B  #$02      COMM
AND MODE

2E4C E7 02            STA B  2,X
2E4E 6F 01            CLR    1,X
2E50 C6 FF            LDA B  #$FF      SET
PIA

2E52 E7 00            STA B  0,X       FOR
OUTPUT

2E54 C6 2C            LDA B  #$2C
2E56 E7 01            STA B  1,X       HAND
SHAKE

2E58 A7 00            STA A  0,X       COMM
AND

2E5A A6 00            LDA A  0,X       STRO
BE IT

2E5C 6F 01     DSTAT  CLR    1,X
2E5E 86 03            LDA A  #$03      STAT
 MODE

2E60 A7 02            STA A  2,X
2E62 6F 00            CLR    0,X
2E64 C6 2C            LDA B  #$2C
2E66 E7 01            STA B  1,X
2E68 A6 00            LDA A  0,X
2E6A 39               RTS
```

Continued on next page

Listing 1, continued:

```
               *
               * READ BY ID
     2E6B      DIPLR  EQU    *
2E6B CE 2EA0   DRDYR  LDX    #DRMSG
2E6E BD E07E          JSR    PDATA1
2E71 BD E1AC          JSR    INEEE
2E74 84 0F            AND A  #$0F
2E76 48               ASL A

2E77 48               ASL A
2E78 BD 2E47          JSR    DCOMM      TRAC
K

2E7B 86 01            LDA A  #$01
2E7D BD 2E47          JSR    DCOMM
2E80 86 01            LDA A  #$01       SET
DATA LINE

2E82 A7 02            STA A  2,X
2E84 8E 1FFF          LDS    #$1FFF
2E87 C6 00     DMORE  LDA B  #$00
2E89 6D 02     DFWAIT TST    2,X
2E8B 2B FC            BMI    DFWAIT
2E8D A6 00            LDA A  0,X
2E8F 36               PSH A

2E90 5A               DEC B

2E91 26 F6            BNE    DFWAIT
2E93 BF 2E9E          STS    DTEMP
2E96 2A EF            BPL    DMORE
2E98 8E A042          LDS    #$A042
2E9B 7E 2ED8          JMP    DTERM
               *
2E9E 0000      DTEMP  FDB    00
2EA0 49        DRMSG  FCC    /ID-/
2EA3 04               FCB    $04
               *
               * DISK IPL WRITE
     2EA4      DIPLW  EQU    *
2EA4 CE 2EA0   DRDYW  LDX    #DRMSG
2EA7 BD E07E          JSR    PDATA1
2EAA BD E1AC          JSR    INEEE
2EAD 84 0F            AND A  #$0F
2EAF 48               ASL A

2EB0 48               ASL A

2EB1 BD 2E47          JSR    DCOMM
2EB4 86 21            LDA A  #$21
2EB6 BD 2E47          JSR    DCOMM
2EB9 6F 01            CLR    1,X
2EBB 86 FF            LDA A  #$FF
2EBD A7 00            STA A  0,X
2EBF 86 2C            LDA A  #$2C
2EC1 A7 01            STA A  1,X
2EC3 6F 02            CLR    2,X
2EC5 CE 1FFF          LDX    #$1FFF
2EC8 A6 00     DWLOOP LDA A  0,X        GET
DATA

2ECA F6 8002   DWFWT  LDA B  DPIA+2
2ECD 2B FB            BMI    DWFWT      WAIT
 FOR FLAG

2ECF B7 8000          STA A  DPIA
2ED2 F6 8000          LDA B  DPIA
2ED5 09               DEX

2ED6 26 F0            BNE    DWLOOP
2ED8 86 83     DTERM  LDA A  #$83       TERM
 FUNCTION

2EDA BD 2E47          JSR    DCOMM
2EDD 6D 02     DTWAIT TST    2,X
2EDF 2B FC            BMI    DTWAIT
2EE1 BD E0BF          JSR    OUT2H
2EE4 7E 2E00          JMP    DCNTRL
                      END               DCNT
RL

MIKBUG E0E3
PDATA1 E07E
INEEE  E1AC
OUTEEE E1D1
OUT2H  E0BF
DPIA   8000
DCNTRL 2E00
DCSTRT 2E27
DCREAD 2E2A
DCWRIT 2E2D
DCEXIT 2E30
DCMSG  2E33
DINIT  2E38
DCOMM  2E47
DSTAT  2E5C
DIPLR  2E6B
DRDYR  2E6B
DMORE  2E87
DFWAIT 2E89
DTEMP  2E9E
DRMSG  2EA0
DIPLW  2EA4
DRDYW  2EA4
DWLOOP 2EC8
DWFWT  2ECA
DTERM  2ED8
DTWAIT 2EDD

TOTAL ERRORS 00000
```

existing programs is allocation of contiguous disk space to a given file. This type of allocation has the disadvantages of needing a disk clean up routine to compact unused space and also results in more wear at the beginning of the disk but is much easier to develop than a system which allows allocation by sectors or pages. Because of the relative ease of implementation the following ideas are based on the contiguous allocation design.

Disk Directory

Track 0 should contain a directory of all the files on the disk. I think the following information should be contained in each disk directory entry:

- **File Name:** 1 to 6 character name used to locate the file.
- **Type:** An indicator to show if the file is a source program, an absolute object program, etc.
- **BOE:** Beginning of extent. The track and sector where the first record of this file is located.
- **EOE:** End of extent. The last track and sector which is allocated to this file.
- **EOD:** End of Data. The last track and sector of the file which contains actual data. The space from **EOD** to **EOE** is for file expansion.
- **Delete Flag:** Indicates that this file has been deleted. This is used by the compaction routine to compress out released space.
- **Creation of Date and Time:** This information is optional but space should be allocated for it in case it is added at a later date.

All of this directory information could be easily contained in 32 bytes with space left over for expansion. This would result in four directory entries per sector or 104 files per disk if all of track 0 were used to contain this information. Actually, sector 1 of track 0 should be reserved for disk header information and pointers, thus leaving 25 sectors or 100 entries.

Disk Utilities

The following utility routines are necessary to manage the disk system.

- **List Directory:** This program lists directory entries so that the user can determine what is on the disk and perform any desired housekeeping.
- **Define or Delete File:** This program allows the user to delete an existing file (ie: set the delete flag in the directory) and to define the characteristics (name, size, type) of a new file.
- **Pack Disk:** This utility moves files so that all allocated disk space is contiguous and updates the file directory, removing the entries for deleted files. When this operation is completed all free disk space is at the end of the disk.
- **Copy File:** Performs a disk to disk copy or a load from tape to disk or save from disk to tape.

Disk IO Subroutines

The following subroutines must be made available to the applications programs to perform disk IO.

- **OPEN:** Sets up IO information about the file.
- **CLOSE:** Deactivates the file and updates the directory entry to indicate any change.
- **READ:** Transfer a file block to memory.
- **WRITE:** Transfer a file block to disk.
- **POS:** Position a file to a specified file block.

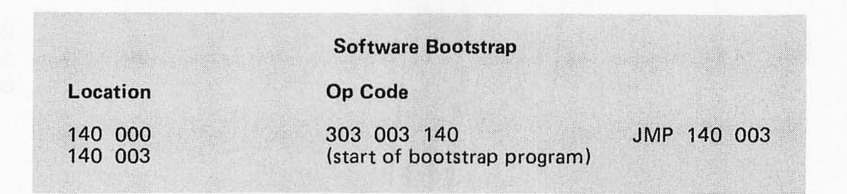
File Control Block

This is a table which is used to maintain current information about a file while it is being used (open). This table is generated at the time a file is opened. At close time, it is used to furnish the necessary information to update the file directory.

Operation Control Block

This is a packet which is created by the applications program to tell the disk IO handler what operation is desired and on what file. Error status can be returned to the application by the disk IO handler in this block.

These are all the basic pieces necessary to put together a disk operating system. Once this is accomplished the applications programs must be modified to use these new IO routines. If all this sounds like a lot of work, it is; but when you have all this completed and debugged you should know everything about 6800s and disk IO. In fact you have learned so much you can start over and do it so much better. Thus, on goes the endless saga of system software. ■



Software Bootstrap

Location	Op Code	
140 000	303 003 140	JMP 140 003
140 003	(start of bootstrap program)	

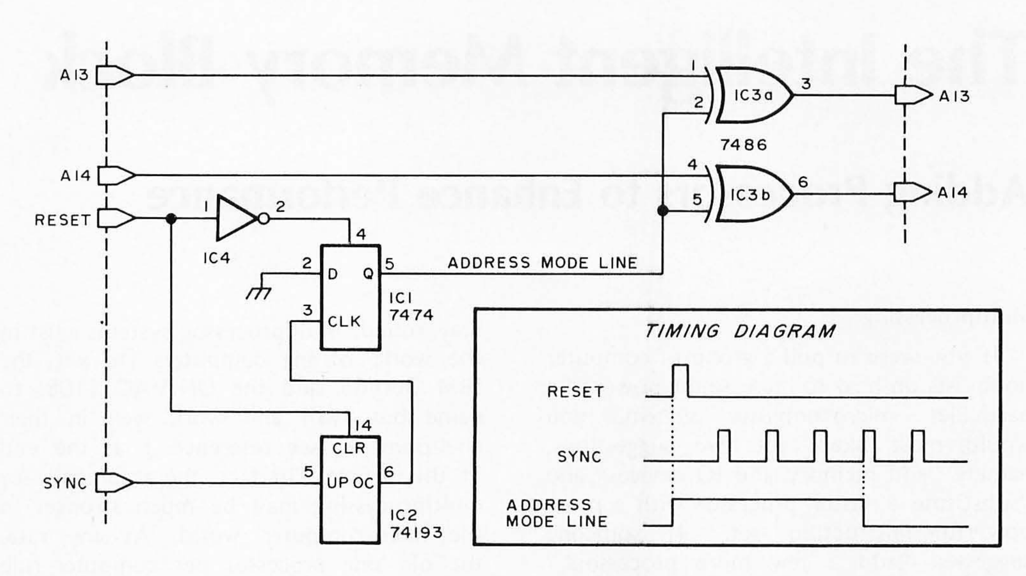


Figure 1: A circuit designed to allow programmable memory to reside at location 0 in an 8080's memory address space, while still allowing a ROM bootstrap permanently in memory. Following system reset, this simple circuit forces the system's address lines to map location 0 into location 140 000 for the first instruction's execution. If the first instruction is a jump to locaton 140 003, the bootstrap can be initiated at 140 003 by an RST 0 instruction forced onto the data bus during the system reset process. (Addresses other than 140 000 can be assigned to the bootstrap ROM with appropriate modifications of the decoding circuit.)

IC Number	Description	+5 V Pin	Gnd Pin
IC1	7474	14	7
IC2	74193	16	8
IC3	7486	14	7
IC4	7404	14	7

Table 1: Power wiring table for figure 1. Note that as usual ceramic bypass capacitors of several tenths of a microfarad should be used as noise suppression, wired between +5 V and ground.

Get On at the Right Address

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The 8080 processor "wakes up" at 000 000 (split octal) as people with homebrew systems probably know. My system has a bootstrap programmable read only memory which initializes my IO ports (keyboard, cassette interface, and video display) and allows me to load a program. Many available programs originate at 000 000 and, although they can be relocated, it is more convenient to leave them. Also, the very useful instruction RST (restart n) makes use of memory originating at 000 000, and, to be effective for different programs, this memory must be programmable. The problem is to get to the bootstrap first, but reserve programmable memory starting at 000 000 for programs.

The following simple circuit allows an immediate software jump to some other memory location besides 000 000 (in this circuit it is 140 000) where the bootstrap is located. Programs can then be loaded into programmable memory starting at 000 000. Note that, after the first instruction is executed, addressing returns to normal in every respect (until another system reset).

The circuit is based on two exclusive OR gates. While the address mode line is high, address lines 13 and 14 will be inverted. This happens at system reset (power on, for instance). At this point the 74193 begins counting SYNC pulses (one every machine cycle) and at the beginning of the fourth machine cycle, clocks a low onto the address mode line, thereby restoring normal addressing. In effect the processor is putting out address 000 000, but the memory interprets it as 140 000. The bootstrap programmable read only memory instruction to jump to 140 003 is at this location. A JMP instruction takes three machine cycles so that, just as the second machine instruction is beginning, addressing returns to the normal mode and you're on your way starting at 140 003.■

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The Intelligent Memory Block

Adding Processors to Enhance Performance

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Multiprocessing

If you were to poll a group of computer hobbyists on how to increase the power of a particular microcomputer system, you would most likely get two suggestions, namely "add memory and IO devices" and "substitute a faster processor with a more powerful instruction set." If someone suggested "add a few more processors," he/she might draw stares of disapproval. However, the idea is not as farfetched as it may sound. Multiprocessor systems exist in the world of big computers (to wit, the IBM 360/65 and the UNIVAC 1108, to name but two) and work well in their environment (see reference 1 at the end of this article). In fact, the arguments for multiprocessing may be much stronger in the microcomputer world. At any rate, the old one processor per computer rule needs reexamination in light of the availability of $20 processor chips.

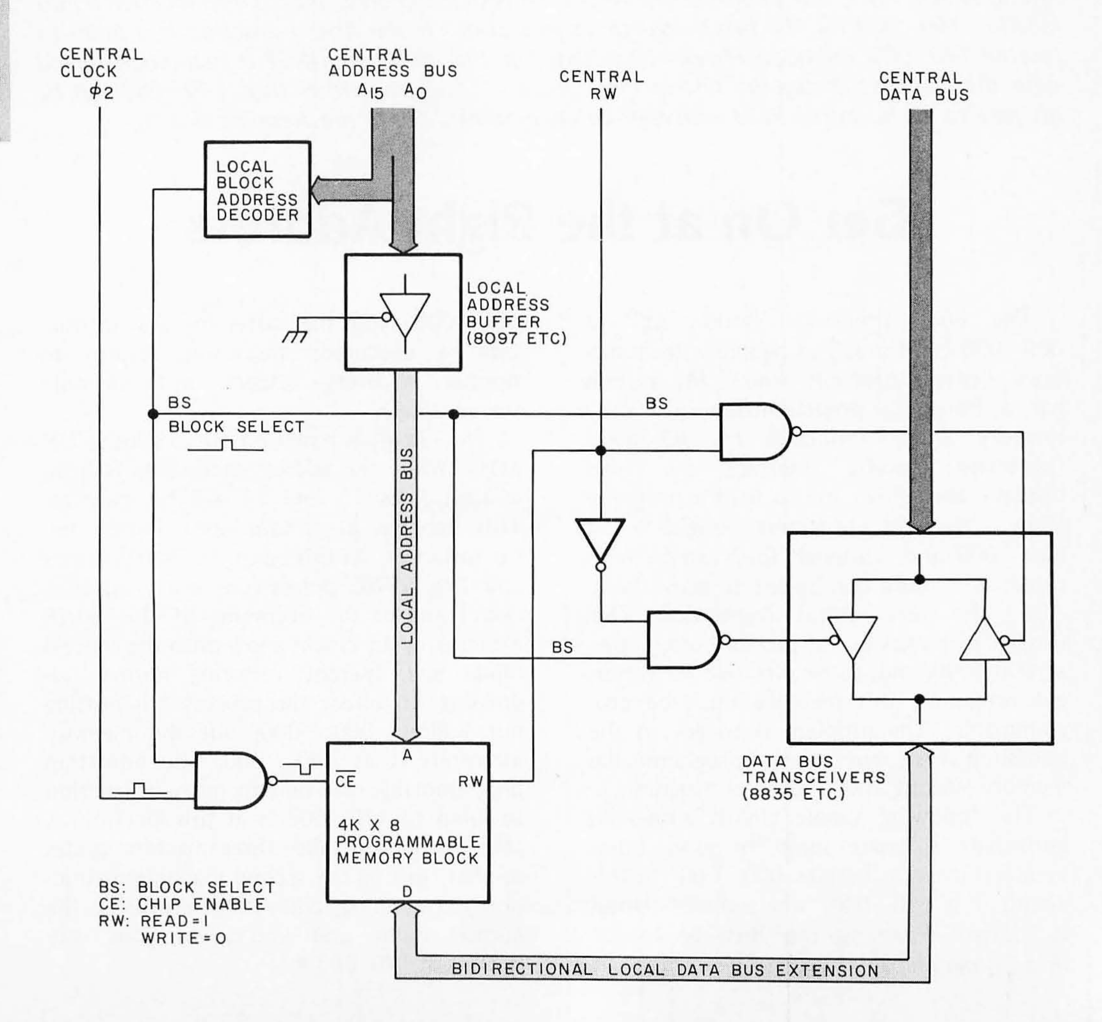


Figure 1: The typical "dumb" memory block. This diagram shows various address decode and control logic elements of a bus oriented computer's 4 K memory block. (The same general diagram would apply as well to an 8 K, 16 K, 32 K or 2 K block.)

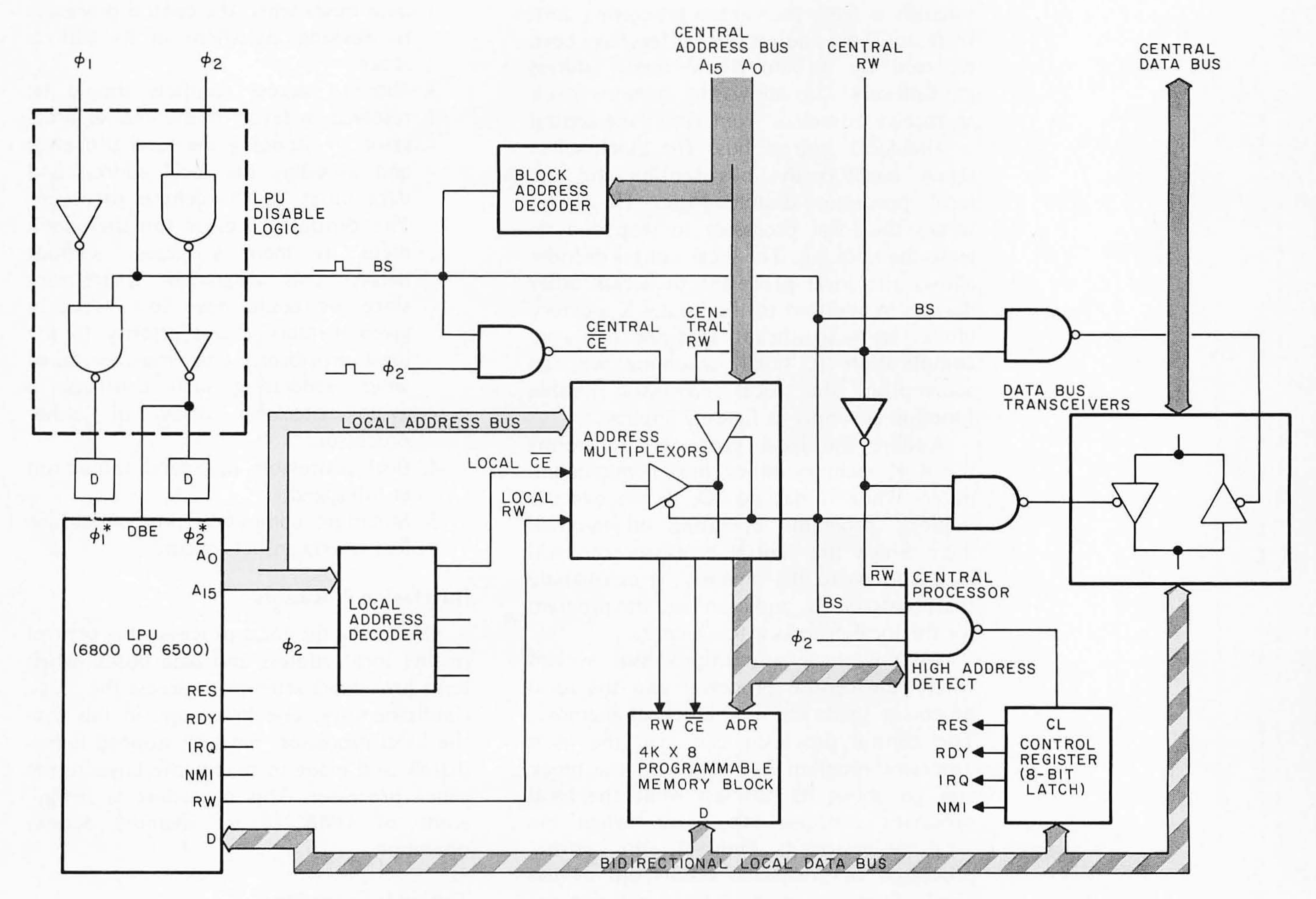
The Dumb Memory Block

Suppose you find the need to add a 4 K by 8 bit block of solid state memory to your microcomputer. Currently available kits cost from $80 to $150 for a system with static memory and buffered buses. Notice that adding a $20 microprocessor to the 4 K memory block represents only about a 20% increase in parts costs. This article examines how one can transform a dumb memory block into a slave computer simply by adding a microprocessor (and a few dollars worth of TTL logic) to the board.

Figure 1 diagrams a typical 4 K by 8 bit programmable memory block. The block address decoder raises the BS (block select) line, enabling the board whenever the four high order address bits from the

About the Author

Ken Castleman has a PhD in electrical engineering and works at the Jet Propulsion Laboratory in Pasadena CA. His professional specialty is digital image processing, with emphasis on medical images. However, microcomputing is one of his hobbies and, since 1973, he has built five microcomputers, three of which were his own design. This article was motivated by a profound philosophical belief that multiprocessor systems have a role to play in the future of microcomputing but that development in this field is currently lagging.



D = CLOCK DRIVER (6800)

*HIGH LEVEL INPUTS (NOT TTL COMPATIBLE)

BS: BLOCK SELECT
RES: RESET
RDY: READY
IRQ: INTERRUPT REQUEST

DBE: DATA BUS ENABLE (6800 ONLY)
CL: CLOCK INPUT
RW: READ=1, WRITE=0
NMI: NON-MASKABLE INTERRUPT

CONTROL REGISTER IS LOADED WHEN CENTRAL PROCESSOR WRITES DATA INTO HIGH ADDRESS OF LOCAL PROCESSOR'S 4K ADDRESS BLOCK

Figure 2: The modification of a "dumb" memory block through addition of a second processor and dual port addressing produces an intelligent memory block. Initialization of the additional processor is accomplished by mapping the last address of the 4 K memory block into a hardware control word as well as memory.

processor specify this 4 K block of memory. The address bus buffers and data bus transceivers prevent the memory chips (32 or so of them) from loading down the central buses. A few TTL gates generate the required control signals.

Adding Intelligence

Figure 2 illustrates the addition of an MC 6800 or MCS 6502 microprocessor to the 4 K by 8 bit memory block of figure 1. We shall call this microprocessor the local processing unit (LPU) to distinguish it from the central processing unit. In figure 2 the address bus buffers have been replaced by a bank of 2 input address multiplexers. This allows the memory block to receive addresses from either the central or the local address bus. The block select signal controls the bus routing and the local processor disable logic. The latter forces the local processor to stop and release the data bus. The local address decoder allows the local processor to access other devices in addition to the local 4 K memory block. It is significant that the hardware complication is small, assuming we can accomplish the local processor disable function as simply as figure 2 implies.

Adding the local processor transforms the 4 K memory block into a microcomputer. While it has no IO, it can execute in-block programs operating on in-block data. Since the central processor can still read and write the memory, it can handle the necessary IO, and even load the program for the local processor to execute.

We now have a multiprocessor system where the central processor and the local processor share the 4 K block of memory. The central processor can load the local processor program and data into the block and go about its business while the local processor processes the data. When the local processor is finished, the central processor can read the results out of the block. Proper division of labor between the two processors can produce an extremely effective computer system.

The Chain of Command

Considerable cleverness is required for interfacing the two processors to avoid a hopelessly slow and undebuggable mess. Let us now establish a reasonable set of interface requirements.

1. Local processor operation should be transparent to the central processor. This means the central processor should be able to read and write the intelligent memory block as if it were an ordinary dumb memory block. Thus the central processor software need not take special notice of the intelligent memory block.
2. The local processor should, by default, have control of the local address and data buses when the central processor is working elsewhere in its address space.
3. Memory access conflicts should be resolved in favor of the central processor by stopping the local processor and awarding the local address and data buses to the central processor. The central processor can then complete its memory access without delay. (This assignment is arbitrary since we could have just as easily given memory access priority to the local processor.) Care must be taken when generating such conflicts to avoid excessive delay of either processor.
4. Both processors, in general, should run at full speed.
5. Minimum computing time should be lost when conflicts occur.

Interfacing Processors

Ordinarily the local processor has control of the local address and data buses. When both processors attempt to access the block simultaneously, one processor (in this case the local processor) must be stopped immediately and made to release the buses to the other processor. This procedure is reminiscent of DMA (direct memory access) operation.

Timing Is Everything

The timing of microprocessor operation is controlled by the system clock. We now investigate this area in the hope of finding a resolution for memory access conflicts. The Motorola MC 6800 and the MOS Technology MCS 6502 microprocessors use a 2 phase nonoverlapping clock sig-

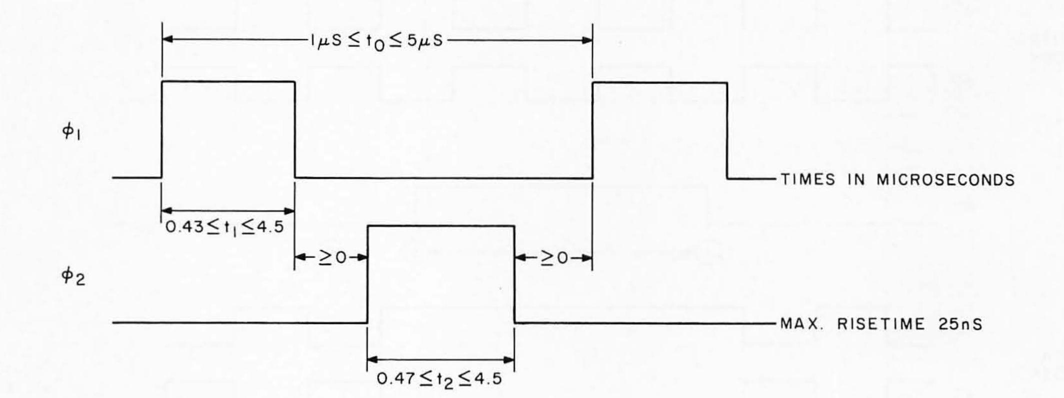


Figure 3: Typical processor clock timing requirements of a 6502 or 6800 processor, abstracted from the specifications documents.

nal to synchronize all data transfers. Figure 3 illustrates the specifications for 6800 and 6502 clock pulses (see references 2 thru 4).

Basically, the microprocessor uses Φ_1 to set up the address and RW lines, and Φ_2 to transfer data to or from the specified address. In a memory read operation the microprocessor puts the address on the address bus during Φ_1 and it remains there throughout Φ_2. During Φ_2 the memory responds by putting eight bits on the data bus. The data is latched into the microprocessor at the fall of Φ_2. For memory write operations the address is set up during Φ_1 as before, but this time the microprocessor puts eight bits on the data bus during Φ_2. The byte is latched into memory at the fall of Φ_2.

Both operations may be summarized as follows. First, the microprocessor updates the address lines about 200 to 300 ns into Φ_1 and the address is stable throughout Φ_2. Secondly, the memory has the rest of Φ_1 and all of Φ_2 to decode the address and the RW line and either put a byte on the data bus or prepare to accept a byte which the microprocessor puts on the bus at the beginning of Φ_2. Finally, the actual data transfer occurs at the fall of Φ_2 when the byte on the data bus is latched into the microprocessor or the memory.

Marking Time with a Rubber Ruler

Getting back to the problem of establishing an interface between the central processor and the local processor, suppose we run both clocks in synchronization. Notice that conflicts will appear during Φ_1 when the central processor sends out an address inside the local block (BS = 1). At this point the local processor must be stopped immediately. Since the READY line cannot accomplish this during write operations we need another solution.

Notice in figure 3 that Φ_1 has 4.5 μs as an upper limit on its duration. No law requires all Φ_1s to be the same length. We can hold the local processor in Φ_1 for up to 4.5 μs if we choose. Thus, we can resolve our conflicts with "clock stretching" (see references 4 and 5). We can hold the local processor in Φ_1 and take it off the buses until the central processor is finished accessing the block. At that point we allow the local processor to go on into Φ_2 and continue its operation. This is particularly nice since conflicts also go away during Φ_1 when the central processor addresses a location outside the local block. As soon as the conflict terminates we can put the local processor back on the buses and let its clock continue in phase with the central processor clock. This operation is diagrammed in figure 4 for a conflict lasting two clock cycles.

Notice that we have achieved our stated goals.

1. In operation, the central processor is unaware of the existence of the local processor.
2. The local processor proceeds unmolested when the central processor is working elsewhere in memory.
3. The central processor never has to wait for access to memory.
4. Except during conflicts, both processors run at full speed.
5. The local processor has to wait only while the central processor is actually using the local buses.

Putting It All Together

Referring back to figure 2, we see that when the four high order address bits select the local block, the local processor

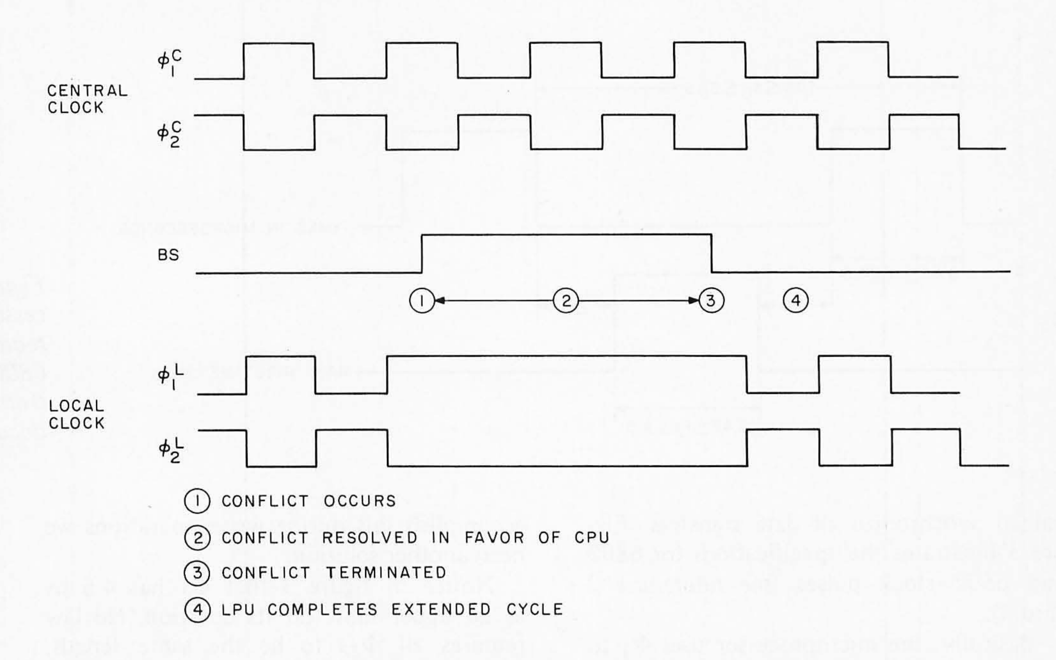


Figure 4. Resolving a conflict by the method of clock stretching. In a 2 processor system built with the 6502 or 6800, lack of a memory wait facility requires substitution of a clock stretching method of direct memory access. Here during the asserted state of the BS (block select) signal, the local processor (L) has its clock stretched while memory is accessed by the central processor (C).

disable logic freezes the local processor in Φ_1. The multiplexers route the central address bus to the memory while three state bus transceivers route the central data bus. The DBE input makes the data bus float during the stretched Φ_1. [While the 6800 also has a TSC (three state control) input which makes it release the address bus, this input acts too slowly (700 ns) for our purposes.] Anyway, only a few gates are required to generate control signals, and the interface is established at little increase in total cost.

Exerting Some Control

Something has to start the LPU and attend to its hardware control functions. A sense of universal justice suggests we should put the central processor in control since it already has its own IO and startup capability. In figure 2 the control register is an 8 bit latch which allows the central processor to supply hardware control signals to the local processor. The central processor can address the control register as the highest byte in the block. When the central processor writes the high byte of the local memory block it simultaneously sets up the control register. The local processor can modify this byte of local memory but not the control register. Either processor can, of course, read the byte but neither can read the control register itself.

The control register allows the central processor to RESET, HALT and INTERRUPT the local processor at will. The RESET function is useful for initiating program execution after the local processor program is loaded. Coming out of RESET, the local processor vectors to a starting address stored at the top of its address space (see references 3 and 4). The NMI and IRQ interrupt lines of the local processor can also be commanded by the central processor through this control word.

Communicating and Cooperating

We must now establish a protocol for communication between central processor software and local processor software. Suppose we wish the local processor to handle mathematical jobs (such as floating point arithmetic, transcendental functions, etc) or perhaps to update in real time spacecraft position during a complex Star Trek game. Some planning is required to establish an effective division of labor between the microprocessors.

As an example, assume the programmer allocates the local memory block as shown in figure 5. The block is viewed as a contiguous region of 4096 bytes with the top byte dedicated to the central processor's local processor control word as described. The central processor must load the program initially and start the local processor by bringing it out of RESET through the local processor control word. Then the local processor might execute a loop checking specified locations allocated to requests looking for pre-established processing request codes from the central processor. When the central processor wants a processing task done it stores the data in the input

Local Block High Address

CONTROL WORD
LPU PROGRAM
INPUT DATA
OUTPUT DATA
REQUESTS
STATUS
STACK
VARIABLES

Local Block Low Address

Figure 5: Memory allocations within a shared memory block must be understood the same way by software of both the central processor and the local processor. Here we show a schematic representation of a workable allocation scheme for use of the local processor to perform subroutines while the central processor goes about other business. The only position which is fixed in the hardware of the design in figure 2 is use of hexadecimal location nFFF in the 4 K block as a command word.

data area, stores a task request code at the request location, and goes about its business. The local processor soon detects the request and begins program execution to accomplish the task. Periodically the central processor checks the words allocated to status in the local memory block to see if the task has been completed. When the local processor finishes the task it stores a completion code in a status byte. On its next status check the central processor discovers that the task is complete and it can use the output data now available in the output region of the local memory block.

In this context the intelligent memory block looks like a self-executing subroutine. The central processor and local processor programs must, of course, agree upon all request and status codes and upon the locations of all variables used in communication. Care must also be taken to ensure that any central processor access to the local memory does not modify data crucial to the computational tasks of the local processor during its active execution of a task. Other approaches to the communication problem also could be used. For example, the local processor with appropriate hardware could generate a central processor interrupt each time it completes a task. This would relieve the central processor of periodic checks for task completion.

The Danger of Overstretching

The upper limits on Φ_1 and Φ_2 duration quoted in figure 3 exist because the 6800 and 6502 microprocessors are dynamic devices. If the internal registers are not refreshed often enough they forget their data and program execution goes haywire. Thus it is relevant to ask if we are in danger of stretching Φ_1 to the breaking point. First, it is necessary for the central processor program, stack and zero page to be located outside the local block. If a central processor program executes out of the local memory block, the local processor will be locked out much longer than the maximum time limit. If the stack of the central processor is in the local memory block, several operations, such as interrupt service and return from interrupt take too long. The zero page, since it is frequently referenced in many programs as a scratch data area, is similarly not a very good choice. Observing these conditions, a 6800 central processor would never address the local block for more than two consecutive clock cycles with the VMA (valid memory address) output high. Thus at 1 MHz operation, Φ_1 would never be stretched beyond 2.5 μs.

The 6502 has no VMA output and, in the worst case (shift instructions addressing data in an absolute X indexed mode), would access the local block for four consecutive clock cycles (see reference 3). At 1 MHz clock operation this stretches Φ_1 to the legal limit of 4.5 μs. We can circumvent this possibly marginal situation with one of the 6502A parts which can run at speeds up to 2 MHz.

Another Way

For 6800 and 6502 microprocessors there is an alternative memory sharing technique which does not involve clock stretching and results in maximum speed for both processors. This technique is known as clock multiplexing. The central and local processor clocks are run in opposite phase. While the central processor is in Φ_1 the local processor is in Φ_2 and vice versa. Two input multiplexers and data transceivers switch the address and data buses from central processor to local processor and back every clock cycle. This way the memory is always connected to whichever processor is in Φ_2 at the moment. Since data transfers only take place in Φ_2 this is adequate.

Clock multiplexing gives both processors unlimited access to the memory. The only penalty is that faster memory is required for the same clock frequency. Since the memory sees the address only for one Φ_2 period it has less time to prepare for a data transfer.

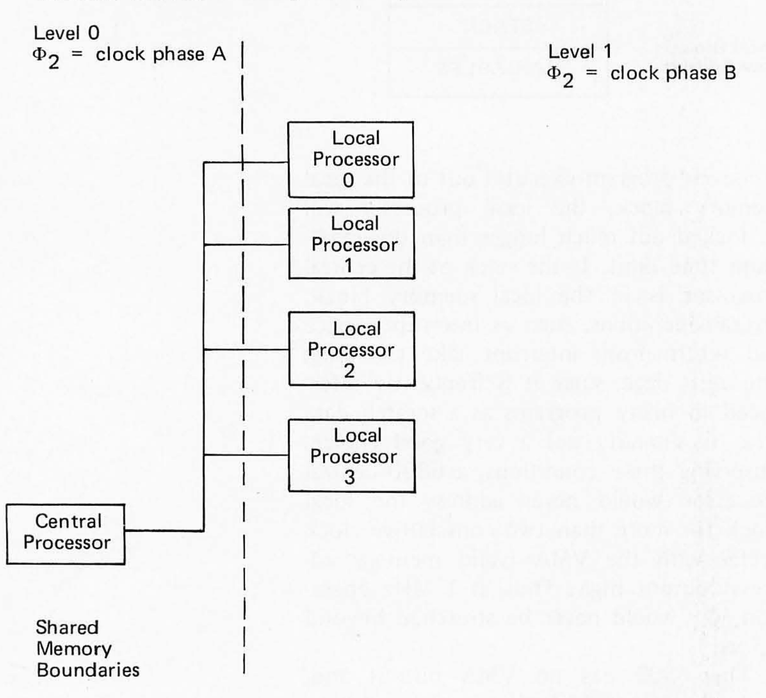
Note that the clock sharing technique can be used to implement multiple processor systems with more than two processors. This is possible if we dedicate one phase of the clock to the central processor, and dedicate an exclusive memory address space region (and the second clock phase) to each local processor. Figure 6 shows a hierarchy diagram of a 5 processor system along with an address space allocation diagram for the central processor. All four local processors use the Φ_2 clock of the central processor as their Φ_1 clock; since the central processor can never address more than one local processor's local memory block at a time, there is never any conflict between local processors.

Getting Fancy

The intelligent memory block is a bona fide microcomputer in its own right. The local processor, with its vast unused address space, is capable of much more than playing butler to the central processor. For example, the local processor could do some external interface job like refreshing a video display or running a multichannel analog IO interface.

Now that we have shed the "one computer-one processor" myth, our horizons have broadened indeed. A 16 K byte microcomputer might just as well have one dumb and three intelligent 4 K blocks as four dumb blocks. What started as an inexpensive way to augment a memory block has landed us knee-deep in exotic computer architecture. Each local processor could even have several sub-local processors working for it in a 3 level architecture, and of course, the possibilities do not end there. At $20 per microprocessor chip, a small computing budget could support a lot of advanced architecture in the family microcomputer. In response to the question "why an intelligent memory block?" one might respond "for twenty bucks, why not?" ■

Hierarchy Diagram of Multiprocessor System



Five Processor Central Processor Memory Address Space Map

Central Processor Hexadecimal Address Range	Contents
0000-00FF	Page 0 scratch area
0100-7FFF	Central processor main memory area which is not shared with local processors. This area contains central processor programs and stack.
8000-8FFF	4 K byte local processor 0 memory overlap region. Address 8FFF is local processor 0 control word.
9000-9FFF	4 K byte local processor 1 memory overlap region. Address 9FFF is local processor 1 control word.
A000-AFFF	4 K byte local processor 2 memory overlap region. Address AFFF is local processor 2 control word.
B000-BFFF	4 K byte local processor 3 memory overlap region. Address BFFF is local processor 3 control word.
C000-FFFF	Spare address space for more local processors and read only memory. Interrupt and reset vectors for central processor at locations FFF8-FFFF.

Figure 6: A multiprocessor system involving more than one intelligent memory block is conceivable. If each intelligent memory block shares a different address space segment with the central processor, and all the intelligent memory blocks (local processors) use an inverted version of the central processor's clock, then there can never be any hardware conflict between operation of the multiple processors. Software considerations as in figure 5 are required to establish consistent communication.

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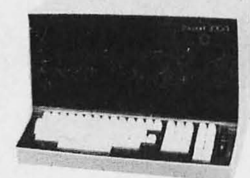
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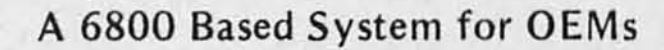
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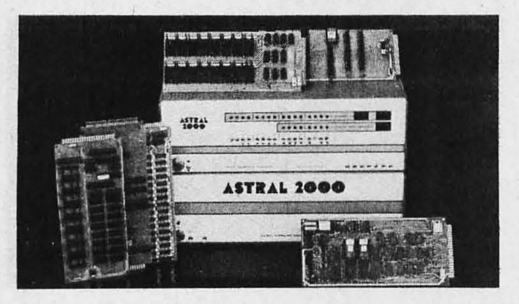


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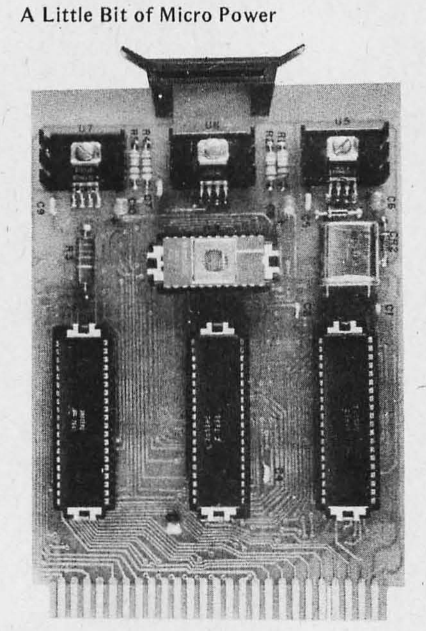
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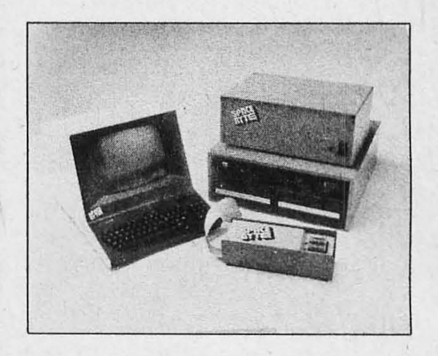
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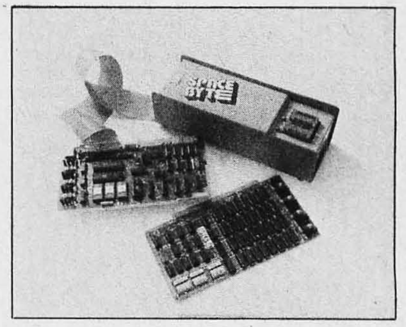


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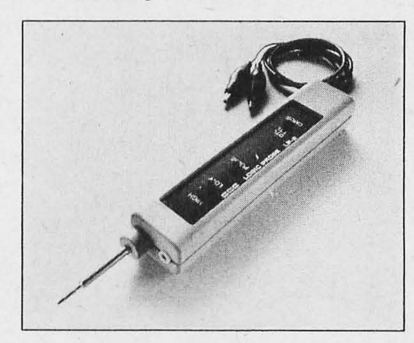
Furniture Designed to Hold Computer Equipment



These desks are specially made to support video displays, terminals, word processing stations and similar equipment. Options such as cutouts for cables, cable channels to eliminate loose cords, pedestals and storage compartments are available. Standard sizes range from 36 inches to 60 inches wide in a variety of colors, from Electronic Systems Furniture Co, 1215 E El Segundo Blvd, El Segundo CA 90245, (213) 322-4612.■

Circle 637 on inquiry card.

Low Cost Logic Probe



This low cost probe features light emitting diodes which indicate high and low logic states and pulses for either TTL or CMOS logic families. Separate dual window comparators drive the high and low LEDs. The pulse detection circuit catches pulses as short as 300 ns with a positive or negative going leading edge. Individual pulses cause the LED to blink for a tenth of a second, while a pulse train flashes it continuously. The probe obtains power from the system under test through a standard phono jack power connector, with a mating cable ending in alligator clips. The probe input impedance is over 300 K ohms. The LP-2 logic probe is $24.95 from Continental Specialties Corp, 44 Kendall St, New Haven CT 06509, (203) 624-3103.■

Circle 638 on inquiry card.

TI's First Personal Computer?



Billed as a "personal computer/calculator," the SR 60A is said to form the heart of a versatile business system that provides the power of a computer with the simplicity of use and low cost of a calculator. The SR 60A uses a microprocessor to control an optional letter quality typewriter and up to two digital cassette drives with file management capability. Serial communications capability also is available. The SR 60A is capable of handling business problems such as inventory, payroll, general ledger, accounts receivable and others. Over 250 programs are available for the machine. Under program control, a small alphanumeric display prompts the user for inputs and performs the calculations, while a 20 character alphanumeric printer can be used to record results. The basic machine provides up to 2640 program steps or 330 data registers, expandable to 7920 program steps or 990 data registers. Prices for the SR 60A start at $1995 from Texas Instruments Inc, Inquiry Answering Service, POB 53 (Attn: SR 60A), Lubbock TX 79408.■

Circle 639 on inquiry card.

Fuel Your Appetite for a 16 Bit System

An 8 page brochure describes the Alpha Micro system, a powerful Altair (S-100) bus compatible package with a timeshared operating system including utilities, a multiuser structured file system with password security, disk file management for floppy or hard disks, AlphaBASIC extended compiler and reentrant run time software, free form text editor and formatter, multiple pass macroassembler and 16 bit microprocessor with hardware floating point capabilities. The microprocessor is built from the Western Digital WD-16 chip set, also used in the LSI-11. The brochure is available from MicroAge, 803 N Scottsdale Rd, Tempe AZ 85281.■

Circle 642 on inquiry card.

New Test Equipment and Hobby Catalog

This 32 page catalog features a complete line of electronic kits and factory assembled instruments, burglar and fire alarm systems, citizens' band accessories and hobbyist kits. New test instruments include a portable digital multimeter, and function generator, a portable color generator, a digital frequency counter, two new oscilloscopes, a self service tube tester and a digital power supply. New hobbyist products include an ignition and engine analyzer and an alpha brainwave monitor. The catalog is available from EICO Inc, 108 New South Rd, Hicksville NY 11801, (516) 681-9300.■

Circle 641 on inquiry card.

End Stackable Sockets

These low cost sockets can be stacked end to end to build a continuous strip socket. The CS2 line is available in all sizes from 8 to 40 pins, from Circuit Assembly Corp, 3169 Redhill Av, Costa Mesa CA 92626, (714) 540-5490.■

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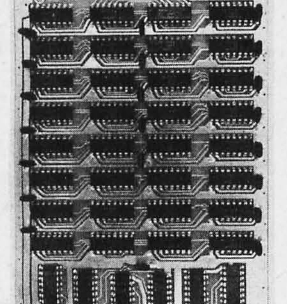
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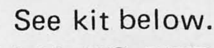
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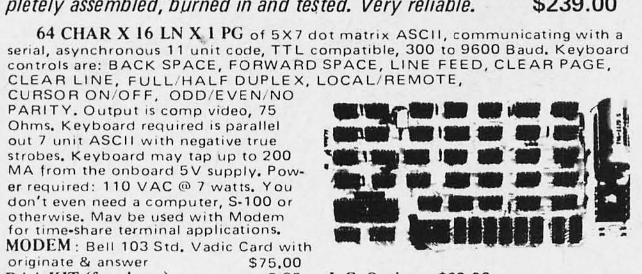
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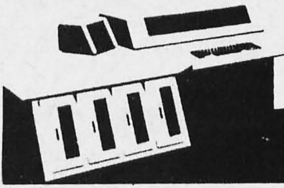
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FD32-1000 (Hard Sector, Inner dia.)			
FD65-1000 (Hard Sector, Outer dia.)			
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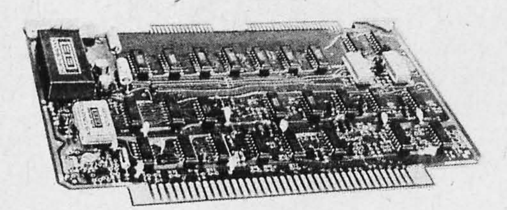
ORDERS NOW BEING TAKEN FOR: THE NOT-SO-DUMB TERMINAL *80 char.X50 ln. rolling full ASCII stand alone communicating Z-80 based terminal. Smarter than the "Owl," includes EBCD to ASCII translator. Options for 256X256 graphics. 100 lines, full editing, etc. Requires KDB and a reasonable monitor such as a slightly modified TV.* $489.00

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What's New?

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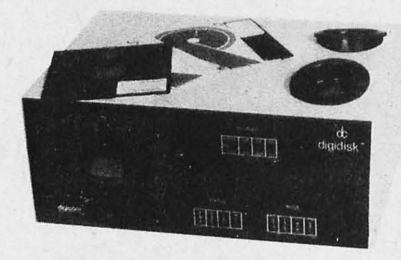
Analog IO for Motorola Exorciser



The MP7400 Analog IO System is electrically and mechanically plug compatible with the Motorola Micromodule and Exorciser microcomputers. Each analog system can accommodate up to 64 single ended or 32 differential input channels and two output channels. A high gain instrumentation amplifier handles input levels as low as 10 mV. The unit interfaces to the microprocessor through a set of memory locations. In single quantities, an input only board with eight differential channels is $295, while a fully loaded board with 32 differential channels and two output channels is $595, from Burr-Brown Research Corp, Intl Airport Industrial Pk, POB 11400, Tucson AZ 85734, (602) 294-1431.■

Circle 631 on inquiry card.

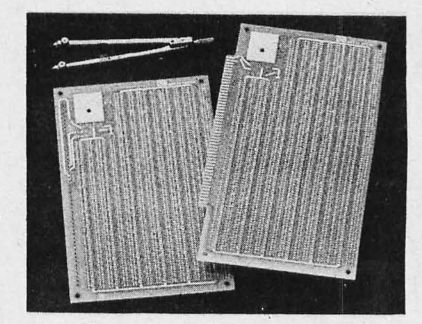
Floppy Disk Emulates Tape



This floppy disk drive and microprocessor based controller is designed to emulate paper tape and magnetic tape. The unit can be used for data collection or offline preparation of messages which can then be transmitted through the optional built in acoustic coupler. The unit will operate with any standard printer or video terminal through an RS232 interface. The program controlling the unit resides on a floppy disk rather than in read only memory, so the system can be easily updated. The Digidisk with RS232 interface is $1199, $1299 with a built-in originate only acoustic coupler, and $1699 with a 1200 bps Bell 202 compatible coupler, from Digicom Data Products Inc, 1440 Knoll Circle, Suite 108, San Jose CA 95112, (408) 279-8711.■

Circle 634 on inquiry card.

New Line of Prototyping Boards



The Before Boards are prototyping boards for the Altair (S-100) bus and the SWTPC (SS-50) bus, offered both with and without a regulated power supply circuit. The S-100 Before Board is supplied with a 100 pin edge connector and can accommodate 56 14 pin or 50 16 pin dual inline packages, and has an extra wide A row to accommodate .4 to .6 inch wide packages. It includes the power supply circuit and is priced at $29.95. The S-100x version of the board omits the power supply circuit for $28.45. The 6800 Before Board is designed to be used with 50 pin Molex connectors and is priced at $23.95, while the 6800x version, which omits the power supply circuit, is $22.46. The boards are available from Multi-Tek Inc, POB 201 Union Square, Milford NH 03055, (603) 673-5011.■

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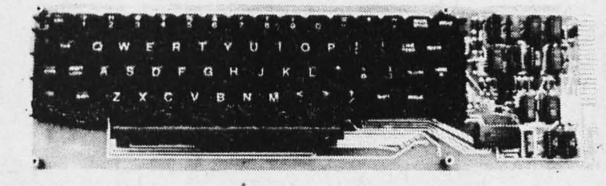
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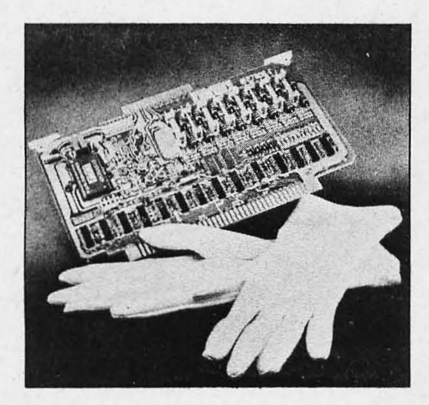
- Metal Enclosure (Painted IBM Blue and White) $25.00
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KIT Includes: Keyboard, P.C. Board, all required components & assembly manual.

NOTE: If you have this 63 Key Teletype Keyboard you can buy the Kit without it for only $44.95

Circle 45 on inquiry card.

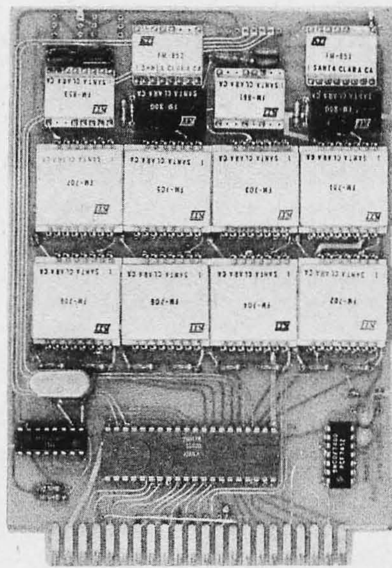
Industrial Quality Analog Input Systems



These analog input systems for Motorola microcomputers offer 12 bit resolution on digital conversion and better than .025% full scale range throughput accuracy. The boards feature input and overvoltage protection and excitation and bridge circuitry. The model MP7608 provides eight differential input channels which accept signals ranging from ± 10 mV to 5 V, while the model MP7608-I is a current input system designed to interface to 4 to 20 mA current loop signals. Both are priced at $595 in single quantities, from Burr-Brown Research Corp, Intl Airport Industrial Pk, POB 11400, Tucson AZ 85734, (602) 294-1431.■

Circle 636 on inquiry card.

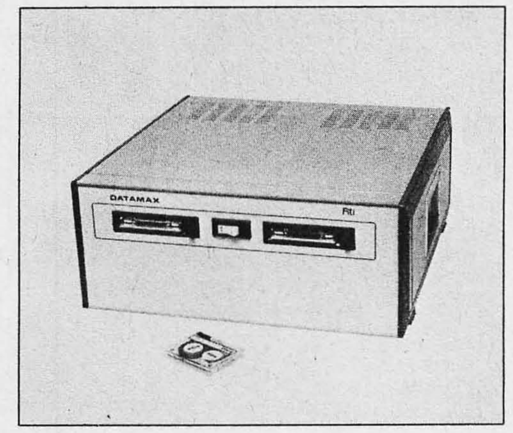
Bidirectional Telephone Interface for 6800 Systems



This touch tone transmit module contains a central office quality tone transmitter and receiver and is suitable for applications such as automatic dialing and receiving and automatic credit card verification. The module is built on an industry standard 4.5 by 6.5 inch 44 pin printed circuit board and is priced at $1499 in single quantities, from Wintek Corp, 902 N 9th St, Lafayette IN 47904, (317) 742-6802.■

Circle 632 on inquiry card.

Cartridge Tape System for Intel MDS and SBC 80 Users



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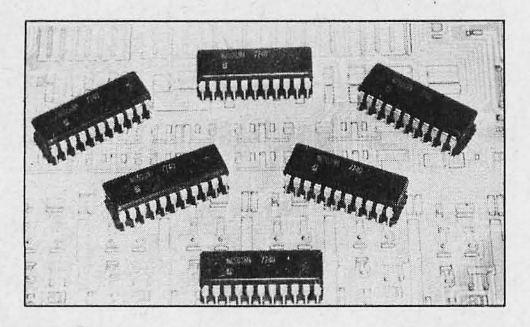
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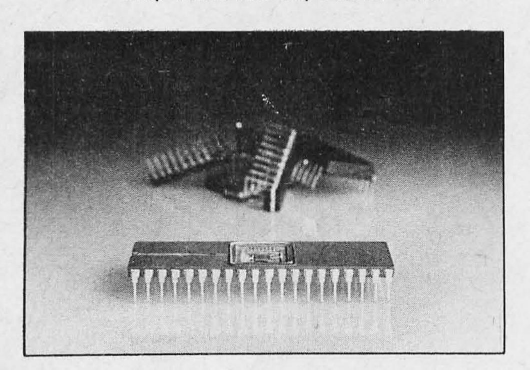
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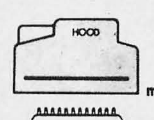


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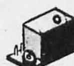
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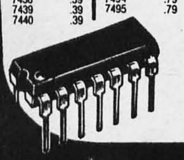
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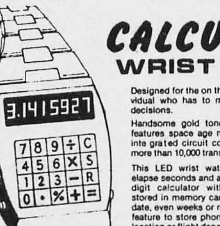
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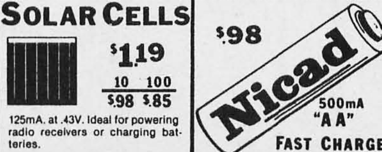
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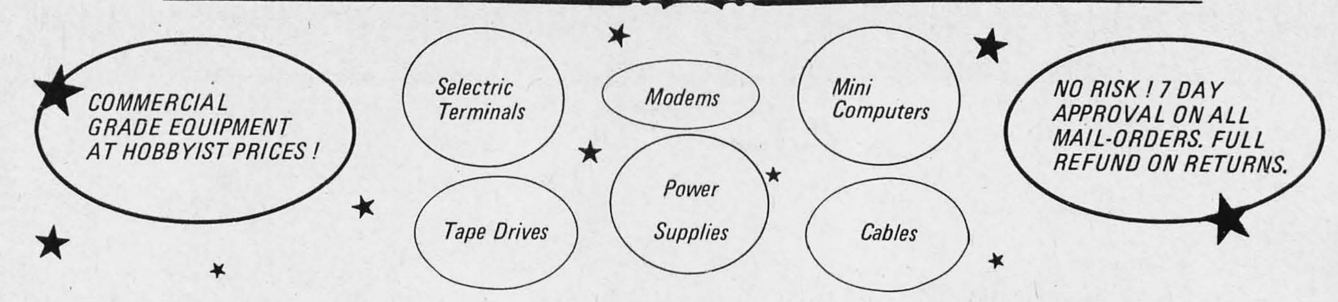
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Circle 13 on inquiry card.

Circle 88 on inquiry card.



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- Also 202-type modems, some with reverse chanel transmission and/or auto answer features.
- Telephone Coupler $ 25

★ ★ ★

AMPEX MODEL TMX TAPE DRIVES with built-in NRZI formatter, 800 BPI, 9 track, 12 IPS, 8" reel includes 8 bit CPU controller diagram and 8080 interface instructions. Ideal for microcomputerist who wants back-up mass storage and access to IBM-type systems via standardized ½" mag tape. $750

POWER SUPPLIES (from Diablo HyType I Terminal): pot adjustable, OV protect. Inputs: 110 or 230 VAC; Outputs: +5V reg. @ 30A; ±15V reg. @ 7A; -9V @ 5A (adjustable to -12V); unreg. +5V (adj. to + 12V): $75

PAPER TAPE READER (Addmaster 601-1): 50 cps, LED sensors read 5-8 level tapes, bidirectional stepper motor, includes TTL serial interface plus 8080 parallel interface instructions. Requires +5V & +24V: $90

INTERDATA Model One 8 Bit **MINICOMPUTER**, includes full front panel, 4K core memory (16K addressable), plug-in teletype port, plus software: $300

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EPOXY CASE AXIAL LEADS
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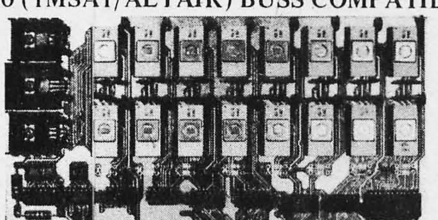
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IMAGINE HAVING 16K OF SOFTWARE ON LINE AT ALL TIME!

KIT FEATURES:
1. Double sided PC Board with solder mask and silk screen and Gold plated contact fingers.
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3. **All** address lines and data lines buffered!
4. All sockets included.
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USES 2708's!

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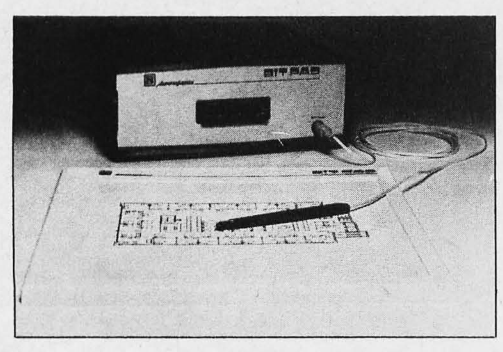
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What's New?

PERIPHERALS

A Pad for Your Bytes



Summagraphics Corporation has announced the Bit Pad data tablet, a new input peripheral designed specifically for small system users.

The unit is designed for fast data collection of X, Y values. The small size (11 by 11 inches, 27.9 x 27.9 cm) and compact design make the Bit Pad portable and adaptable to a variety of applications. It can be interfaced to any microcomputer using its standard 8 bit parallel output.

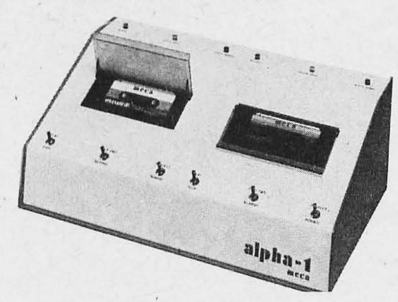
Applications include medical treatment, opinion sampling, education, real estate, design, games, research, computer animation and so on.

It can be used as a variable keyboard for menu picking, for inputting data for inventory control or parts programming, etc. The price is $555.

Contact Summagraphics Corporation, 35 Brentwood Av, Fairfield CT 06430, (203) 384-1344.■

Circle 584 on inquiry card.

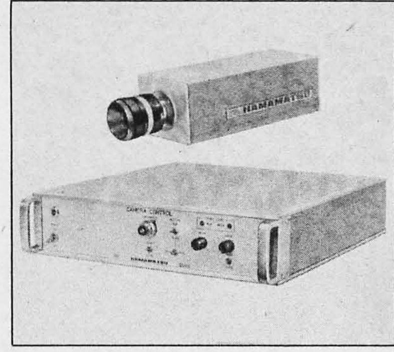
Digital Cassette Drives for Radio Shack TRS-80 and Altair (S-100) Bus



This cassette based mass storage system is offered in two versions for popular personal computers. Pictured is the Alpha 1 system for Altair (S-100) bus computers. The controller card plugs into the bus, controls up to four drives and will bootstrap from tape without the need for a read only memory monitor. A stand alone cassette operating system or a system with extended BASIC is available for the Alpha 1. Prices start at $240. The CMS system is said to be plug compatible with the Radio Shack TRS-80 computer, with prices starting at $399. Each cassette drive can store up to 500 K bytes and can record or play back information at 780 bytes per second (data rate 6250 bps). Average access time to information anywhere on the cassette is 17 seconds. The units are available from MECA, 7026 Old Woman's Spring Rd, Yucca Valley CA 92284, (714) 365-7686.■

Circle 581 on inquiry card.

Vidicon Camera



The modular C-1000 vidicon camera system has all handshake and control lines for computer interfacing built in. Standard building blocks are available to perform commonly needed functions such as point tracking, area measurement and so on. High resolution (1000 TV lines) and low distortion (less than 0.2%) and drift (less than 0.05% per day) make the unit appropriate for research and industrial computer applications. Prices start at $3500 from Hamamatsu Corporation, 120 Wood Av, Middlesex NJ 08846, (201) 469-6640.■

Circle 582 on inquiry card.

Video Graphics with Plotting Printer

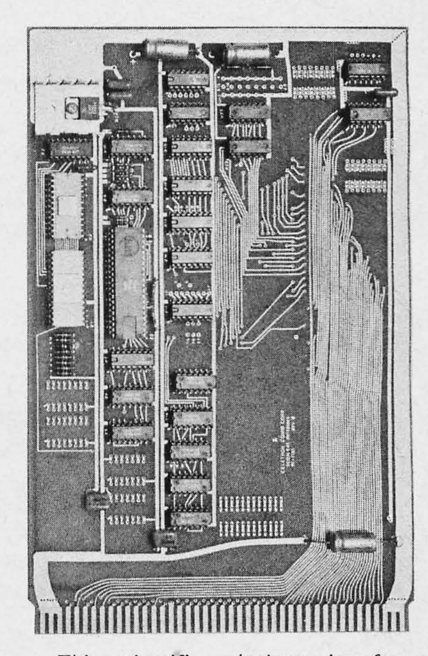




A video graphic display and matching printer with plotting capabilities are now available for the Wang 2200 series computers. The 2282 Graphics CRT has a 12 inch (30.5 cm) diagonal screen with 800 by 512 addressable dots. Vectors are generated by turning on a series of dots approximating a line. The 2231W-3 printer provides an accurate hard copy of a graphics image by printing strips of 800 dots by 8 dots. Alphabetic information can also be printed at 120 characters per second. The 2282 is $3600 and the 2231W-3 is $3800 from Wang Laboratories Inc, 1 Industrial Av, Lowell MA 01851, (617) 851-4111.■

Circle 580 on inquiry card.

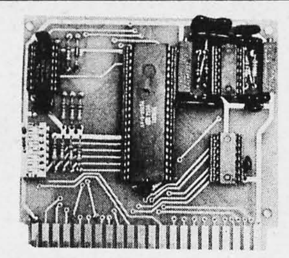
Scientific Calculator Interface



This scientific calculator interface board kit, which includes interface software for 8080 and 6800 based systems, is available in two versions, one for the Motorola Exorciser bus and one for the Altair (S-100) bus. The board employs the MOS Technology 7529-103 programmable calculator chip, which features a full set of mathematical functions, factorials, and up to two levels of parentheses in expressions. The kit is $99.95 from Mini Micro Mart, 1618 James St, Syracuse NY 13204, (315) 422-4467.■

Circle 583 on inquiry card.

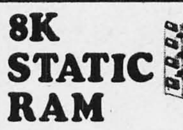
ELECTRONIC SYSTEMS
p.o. box 212 Burlingame CA 94010
(408) 374-5984

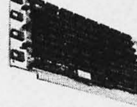


UART & BAUD RATE GENERATOR

Part no. 101
- Converts serial to parallel and parallel to serial
- Low cost on board baud rate generator
- Baud rates: 110, 150, 300, 600, 1200, and 2400
- Low power drain +5 volts and -12 volts required
- TTL compatible
- All characters contain a start bit, 5 to 8 data bits, 1 or 2 stop bits, and either odd or even parity.
- All connections go to a 44 pin gold plated edge connector
- Board only $12.00; with parts $35.00

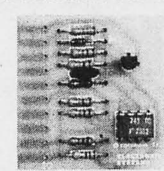
8K STATIC RAM





Part no. 300
- 8K Altair bus memory
- Uses 2102 Static memory chips
- Memory protect
- Gold contacts
- Wait states
- On board regulator
- S-100 bus compatible
- Vector input option
- TRI state buffered
- Board only $22.50; with parts $160.00

RS-232/TTL INTERFACE



Part no. 232
- Converts TTL to RS-232, and converts RS-232 to TTL
- Two separate circuits
- Requires -12 and +12 volts
- All connections go to a 10 pin gold plated edge connector
- Board only $4.50; with parts $7.00

DC POWER SUPPLY

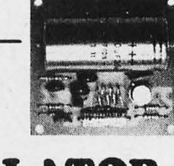
Part no. 6085
- Board supplies a regulated +5 volts at 3 amps., +12,-12, and -5 volts at 1 amp.
- Board has filters, rectifiers, and regulators
- Power required is 8 volts AC at 3 amps., and 24 volts AC C.T. at 1.5 amps.
- Board only $12.50

TIDMA

Part no. 112
- Tape Interface Direct Memory Access
- Record and play programs without bootstrap loader (no prom) has FSK encoder/decoder for direct connections to low cost recorder at 625 baud rate, and direct connections for inputs and outputs to a digital recorder at any baud rate.
- S-100 bus compatible
- Comes assembled and tested for $160.00

TAPE INTERFACE

Part no. 111
- Play and record Kansas City Standard tapes
- Converts a low cost tape recorder to a digital recorder
- Works up to 1200 baud
- Digital in and out are TTL-serial
- Output of board connects to mic. in of recorder
- Earphone of recorder connects to input on board
- Requires +5 volts, low power drain
- Board $7.60; with parts $27.50
- No coils



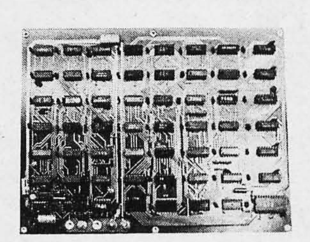
Part no. 107
RF MODULATOR
- Converts video to AM modulated RF, Channels 2 or 3
- Power required is 12 volts AC C.T., or +5 volts DC
- Board $4.50; with parts $13.50

APPLE I MOTHER BOARD



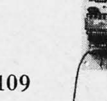
Part no. 102
- 10 slots – 44 pin (.156) connectors spaced ¾" apart
- Connects to edge connector of computer
- Pin 20 and 22 connects to X & Z for power and ground
- Board has provisions for by-pass capacitors
- Board cost $15.00

TELEVISION TYPEWRITER



Part no. 106
- Stand alone TVT
- 32 char/line, 16 lines, modifications for 64 char/line included
- Parallel ASCII (TTL) input
- Video output
- 1K on board memory
- Output for computer controlled curser
- Auto scroll
- Non-distructive curser
- Curser inputs: up, down, left, right, home, EOL, EOS
- Scroll up, down
- Requires +5 volts at 1.5 amps, and -12 volts at 30 mA
- Board only $39.00; with parts $145.00

MODEM



Part no. 109
- Type 103
- Full or half duplex
- Works up to 300 baud
- Originate or Answer
- No coils, only low cost components
- TTL input and output-serial
- Connect 8 ohm speaker and crystal mic. directly to board
- Uses XR FSK demodulator
- Requires +5 volts
- Board $7.60; with parts $27.50

To Order:





Mention part number and description. For parts kits add "A" to part number. Shipping paid for orders accompanied by check, money order, or Master Charge, BankAmericard, or VISA number, expiration date and signature. Shipping charges added to C.O.D. orders. California residents add 6.5% for tax. Parts kits include sockets for all ICs, components, and circuit board. Documentation is included with all products. Dealer inquiries invited. 24 Hour Order Line: (408) 374-5984. E21

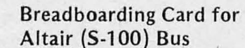
Circle 44 on inquiry card.



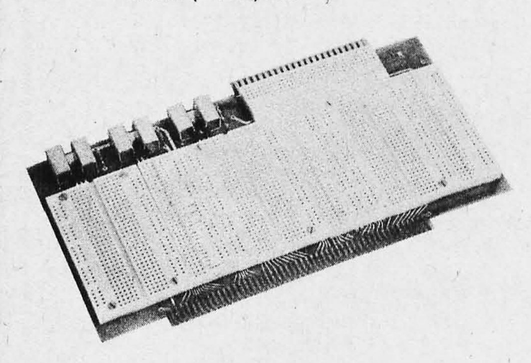
Graphics for Your SOL Computer

This kit adds a 128 horizontal by 48 vertical point graphic display capability to your SOL computer or VDM-1 video display board. A piggyback printed circuit board mounts directly on the SOL or VDM-1 board to add graphics. Software, supplied on a SOL CUTS cassette and paper tape, provides: a driver routine to manipulate individual points, links to the SOL's BASIC 5, demonstration plotting programs and an animation program for John Conway's game of Life. The kit is available for $50 from KEA Micro Design, POB 6531 Station A, Toronto, Ontario CANADA M5W 1X4.■

Circle 604 on inquiry card.



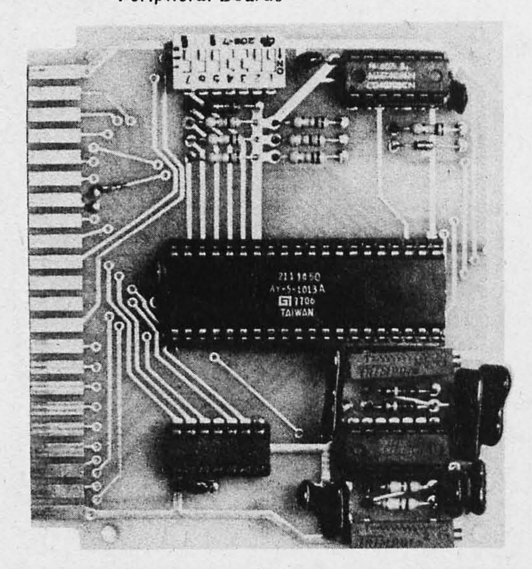
Breadboarding Card for Altair (S-100) Bus



This breadboarding card makes it especially convenient to add experimental circuitry to an Altair (S-100) bus compatible computer. The board plugs into the bus (with offset contacts to prevent incorrect insertion) and provides breadboard access to every signal, divided into address, data and control sections. Voltage regulators for +5 V, +12 V and −12 V are provided as well as points for obtaining unregulated voltage. 22 gold plated contacts are provided on the other side of the card for external connections. Three SK-50 breadboarding sockets, each with 32 pairs of five common contacts and a series of common bus strips are included as well as a breadboarding area for the 22 card edge contacts. The card is priced at $75 from E & L Instruments Inc, 61 First St, Derby CT 06418, (203) 735-8774.■

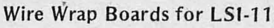
Circle 605 on inquiry card.

A Plethora of Peripheral Boards

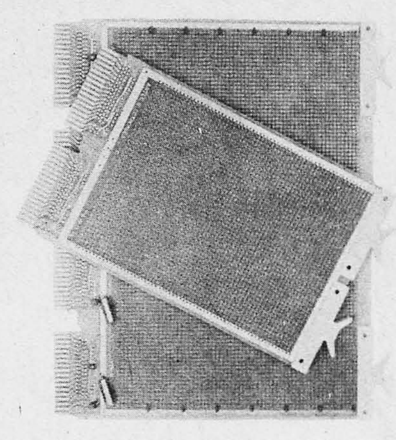


A variety of peripheral boards are now available for the do-it-yourselfer, including a universal asynchronous receiver transmitter (UART) board (pictured), a full duplex, 300 bps modem, a TTL compatible RS232C interface, a Kansas City standard cassette tape interface, a 32 or 64 character per line video display board, and an RF modulator board with power supply to interface a video signal to a television set. Also available are an 8 K byte static memory board for the Altair (S-100) bus, and a mother board, 8 K memory board, and serial IO board for Apple I computers. All circuit boards come with complete instructions and parts lists, and are designed to use inexpensive, easy to find parts. Parts kits and fully assembled units are also available. Prices for the boards range from $5 to under $40, from Electronic Systems, POB 212, Burlingame CA 94010, (415) 573-7788.■

Circle 606 on inquiry card.



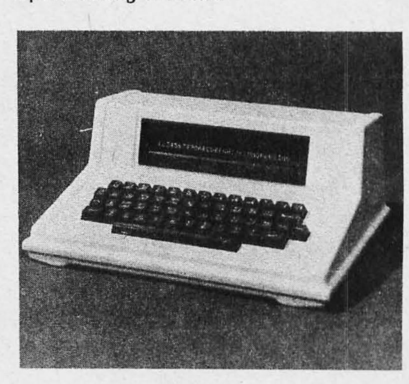
Wire Wrap Boards for LSI-11



These wire wrap boards can be used to build your own memory and input output systems for the LSI-11 computer. Each board, designed for insertion of wire wrap pins, can accommodate about 130 standard 14 pin and 16 pin dual in line packages, plus passive components. A ground shield is provided on one side of the board. The WW-11.5 half size version sells for $35 in single quantities, while the WW-11 full size version is $75, from Artec Electronics Inc, 605 Old County Rd, San Carlos CA 94070, (415) 592-2740.■

Circle 607 on inquiry card.

Space Saving Terminal



The Transactor I data terminal consists of a single line 32 character gas discharge display with a 5 by 7 dot matrix for easy reading, and a 53 key Teletype style keyboard. It can be attached to almost any computer, with an RS232 or 20 mA current loop interface. Switches allow the user to select the operating mode including 110 to 9600 bps data rate, full or half duplex, even, odd or no parity, five to eight data bits, and one or two stop bits.

Lightweight and small, the Transactor is housed in an attractive and sturdy aluminum case that measures only 6 by 15 by 11 inches (15.2 by 38.1 by 27.9 cm). A stylized molded case is available. Price of the standard Transactor I in quantity is $595, from Computerwise Inc, 4006 E 137th Ter, Grandview MO 64030, (816) 765-3330.■

Circle 608 on inquiry card.

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74L$14	.85	74L$125	.46	74L$258	.70
74L$20	.23	74L$126	.46	74L$266	.26
74L$21	.23	74L$132	.75	74L$283	.72
74L$22	.23	74L$138	.70	74L$365	.55
74L$30	.23	74L$139	.70	74L$366	.55
74L$32	.30	74L$151	.65	74L$367	.55
74L$37	.31	74L$153	.66	74L$368	.55
74L$38	.31	74L$154	1.00	74L$386	.39
74L$42	.60	74L$157	$.62	81L$95	.77
74L$47	.75	74L$160	.82	81L$96	.77
74L$48	.72	74L$161	.82	81L$97	.77
74L$73	.35	74L$162	.82	81L$98	.77
74L$74	.35	74L$163	.82		
74L$75	.53	74L$164	.98		
74L$76	.37	74L$174	.75		
74L$86	.36	74L$175	.79		
74L$90	.52	74L$190	.90		
74L$92	.52	74L$191	.90		

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74XX

7400	.11	7441	.70	74100	.28
7401	.13	7442	.37	74107	.28
7402	.13	7443	.59	74109	.22
7403	.13	7444	.59	74121	.29
7404	.15	7445	.65	74122	.38
7405	.13	7446	.62	74123	.48
7406	.16	7447	.59	74132	.65
7407	.23	7448	.60	74141	.70
7408	.17	7450	.13	74145	.65
7409	.17	7451	.13	74150	.88
7410	.13	7453	.13	74151	.61
7411	.18	7454	.13	74153	.61
7412	.13	7460	.14	74154	.95
7413	.25	7470	.26	74157	.55
7414	.61	7472	.21	74161	.55
7416	.24	7473	.21	74163	.55
7417	.22	7474	.27	74164	.85
7420	.13	7475	.45	74165	.90
7423	.25	7476	.28	74170	1.69
7425	.25	7479	5.00	74173	1.10
7426	.22	7480	.31	74175	.85
7427	.17	7481	.95	74175	.75
7430	.13	7482	.50	74176	.69
7432	.23	7483	.62	74177	.70
7437	.21	7485	.75	74180	.65
7438	.21	7486	.26	74181	1.75
7439	.25	7489	1.75	74190	.95
7440	.13	7490	.40	74191	.95
		7491	.51	74192	.79
		7492	.40	74193	.80
		7493	.40	74195	.49
		7494	.60	74221	.86
		7495	.60	74251	1.00
		7496	.60	74365	.62
				74366	.62
				74367	.62
				74368	.62

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1101	.75

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Z-80	24.95
Z-80A	34.95
6800	16.50

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4002	.16	4024	.67
4006	.99	4025	.16
4007	.16	4028	.74
4008	.79	4030	.22
4009	.37	4035	.98
4010	.37	4040	.99
4011	.16	4049	.34
4012	.16	4050	.34
4013	.29	4051	.89
4014	.74	4052	1.15
4015	.74	4053	.89
4016	.29	4066	.59
4017	.79	4071	.19
4018	.79	4081	.23
4019	.23	4082	.23
4020	.84	4507	.39
4021	.89	4510	1.05
4022	.89		

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Kit with Software 174.95
MT-1
15-Slot Mother Board 39.95
XB-1 EXTENDER BOARD
Bare Board 8.99
SSM 8080 MONITOR V1
ON 2-2708 47.00
ON 8-1702A 47.00

BOOKS

Home Computers: 210 Questions and Answers; Volume 1: Hardware by Rich Didday 225 pp.	$7.95
Home Computers: 210 Questions and Answers; Volume 2: Software by Rich Didday 175 pp.	$6.95
Calculator Users' Guide and Dictionary by Charles Sippl 444 pp.	$12.95
Microcomputer Dictionary and Guide by Charles Sippl 704 pp.	$19.95
Introduction to BASIC by Jeffrey Morton 200 pp.	$8.95
Analysis and Design of Digital Circuits and Computer Systems by Paul Chirlian	$22.50
Finite State Fantasies by Rich Didday 50 pp.	$1.25

REGULATORS

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		LM 320K-24	1.75
		LM 320T-5	1.10
LM 309H	1.10	LM 320T-12	1.10
LM 309K	.99	LM 320T-15	1.10
LM 320H-5	1.19	LM 340K-5	.85
LM 320H-6	1.19	LM 340K-8	1.35
LM 320H-8	1.19	LM 340K-12	.85
LM 320H-12	1.19	LM 340K-15	.85
LM 320H-15	1.19	LM 340K-18	1.35
LM 320H-18	1.19	LM 340K-24	.85
LM 320H-24	1.19	LM 340T-5	.95
LM 320K-5	1.35	LM 340T-8	.95
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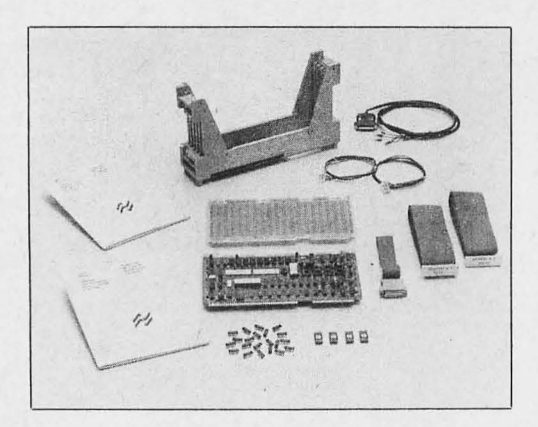
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Prototyping Package for 8080 Systems



Designers can quickly construct custom interface systems using the BLC 80/10 board level computers with the aid of this prototyping package. The BLC 80P package includes a BLC 80/10 computer board with 1 K bytes of programmable memory, a system monitor in 2 K bytes of read only memory, and an additional 2 K bytes of blank 2708 type programmable read only memory. A prototyping board with space for 114 16 pin sockets or an equivalent mix of other sockets is also included. The boards are housed in a four slot card cage which also serves as a backplane and system bus. Two power cables are supplied as well as two 50 conductor ribbon cables for connection to external circuits. The BLC 80/10 has jumper selected options for RS232 or current loop interfaces, and cables are supplied for a CRT terminal and for a Teletypewriter. Documentation includes a hardware reference manual, user's guide and schematics. The BLC 80P is priced at $878 from National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara CA 95051, (408) 737-5166.■

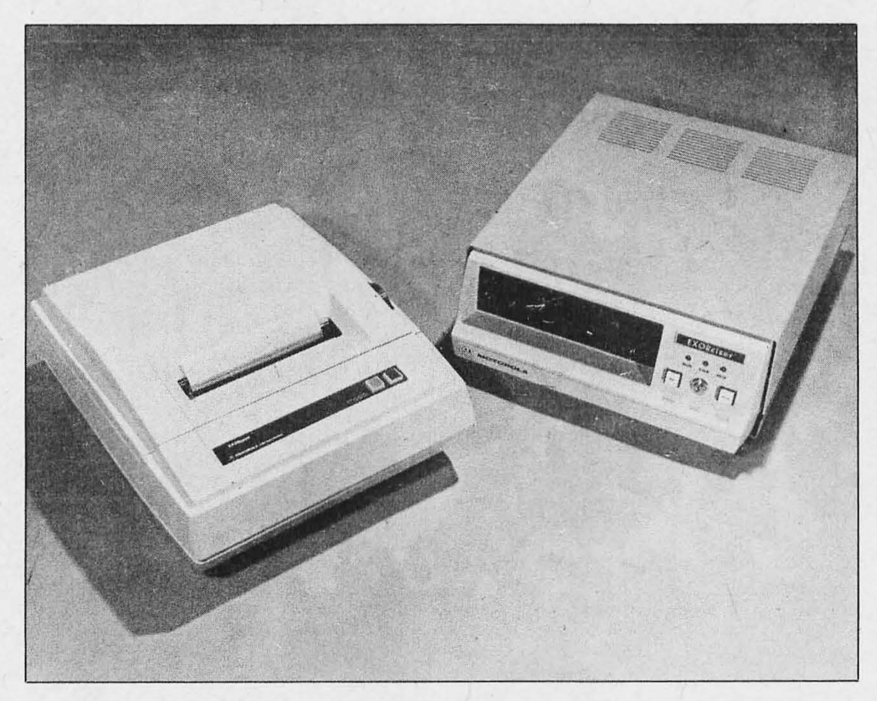
Circle 610 on inquiry card.

Multifunction Floppy Controller for LSI-11

Several common functions have been combined in this dual width interface card for the LSI-11. The interface controls up to three Shugart SA-400 minifloppy drives, provides a direct memory access dynamic memory refresh controller, and includes sockets for up to 4 K or 8 K 16 bit words of programmable read only memory. The floppy controller performs several functions automatically including track seek and verify, cyclic redundancy code generation and checking, and drive motor timeout shutoff. The memory sockets hold up to 4 K of 2708 type chips or up to 8 K of 2716 type chips. The −5 V power supply for these chips is generated on the board. Provisions have been made for mapping the LSI-11 bootstrap addresses onto these chips or onto fusible link read only memories. The MDC11 combined board is priced at $510, the minifloppy drives at $325, the MREF11 dynamic memory refresh controller alone is $195 and the PROM11 read only memory section alone is $170, from Andromeda Systems Inc, 14701 Arminta St J, Panorama City CA 91402, (213) 781-6000.■

Circle 613 on inquiry card.

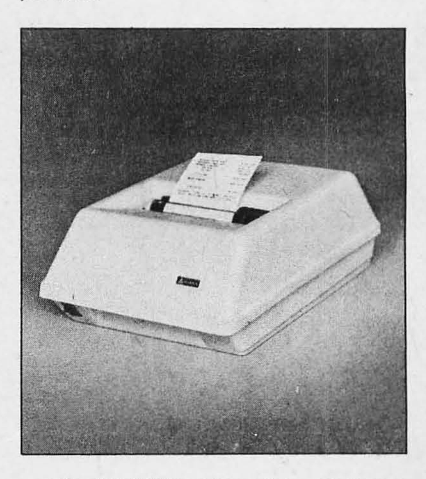
Printer for Motorola Exorciser



Designed for use with the Motorola Exorciser or Micromodules, this impact printer produces lines of up to 80 5 by 7 dot matrix characters at a speed of 110 characters per second (about 65 lines per minute). The print head moves in both directions on 8.5 inch (21.6 cm) wide roll paper and uses a conventional Teletype ribbon. A peripheral interface module and interconnecting cable are included with the printer, making the device functionally equivalent to a Centronics 306 type printer. The MDOS and EDOS operating systems for the Exorciser provide drivers and commands for the new device. A 230 V 50 Hz version is available for European users. The EXORprint printer is $1725 from Motorola distributors or from the manufacturer. Contact Motorola Semiconductor Products Inc, Technical Information Center, POB 20924, Phoenix, AZ 85008, (602) 244-6815.■

Circle 612 on inquiry card.

Printer Offers 6 or 12 Characters per Inch



The DP-1000 series printers feature a dot matrix impact printing element capable of printing 64 alphanumeric and special characters in 40 characters per line at 1.25 lines per second on standard single or multiple copy paper rolls. Three RS232C configurations allow convenient interfacing to most minicomputers, modems and teleprinters. Data rates from 110 to 2400 bps are available. Single or double width characters are selected with an external control line, allowing either 6 or 12 characters per inch to be intermixed on a line. Prices start under $700 with substantial quantity discounts, from Anadex, 9825 DeSoto Av, Chatsworth CA 91311, (213) 998-8010.■

Circle 615 on inquiry card.

DIODES/ZENERS

1N914	100v	10mA	.05
1N4005	600v	1A	.08
1N4007	1000v	1A	.15
1N4148	75v	10mA	.05
1N753A	6.2v	z	.25
1N758A	10v	z	.25
1N759A	12v	z	.25
1N4733	5.1v	z	.25
1N5243	13v	z	.25
1N5244B	14v	z	.25
1N5245B	15v	z	.25

SOCKETS/BRIDGES

8-pin	pcb	.25	ww	.45
14-pin	pcb	.25	ww	.40
16-pin	pcb	.25	ww	.40
18-pin	pcb	.25	ww	.75
22-pin	pcb	.45	ww	1.25
24-pin	pcb	.35	ww	1.10
28-pin	pcb	.35	ww	1.45
40-pin	pcb	.50	ww	1.25

Molex pins	.01	To-3 Sockets	.45
2 Amp Bridge		100-prv	1.20
25 Amp Bridge		200-prv	1.95

TRANSISTORS, LEDS, etc.

2N2222	NPN	(Plastic .10)	.15
2N2907	PNP		.15
2N3906	PNP		.10
2N3054	NPN		.35
2N3055	NPN	15A 60v	.50
T1P125	PNP	Darlington	.35
LED Green, Red, Clear			.15
D.L.747	7 seg 5/8" high com-anode		1.95
XAN72	7 seg com-anode		1.50
FND 359	Red 7 seg com-cathode		1.25

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4001	.20
4002	.20
4004	3.95
4006	1.20
4007	.35
4008	.95
4009	.30
4010	.45
4011	.20
4012	.20
4013	.40
4014	1.10
4015	.95
4016	.35
4017	1.10
4018	1.10
4019	.60
4020	.85
4021	1.35
4022	.95
4023	.25
4024	.75
4025	.35
4026	1.95
4027	.50
4028	.95
4030	.35
4033	1.50
4034	2.45
4035	1.25
4040	1.35
4041	.69
4042	.95
4043	.95
4044	.95
4046	1.75
4049	.70
4050	.50
4066	.95
4069	.40
4071	.35
4081	.70
4082	.45

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7400	.15
7401	.15
7402	.20
7403	.20
7404	.15
7405	.25
7406	.35
7407	.55
7408	.25
7409	.15
7410	.10
7411	.25
7412	.30
7413	.45
7414	1.10
7416	.25
7417	.40
7420	.15
7426	.30
7427	.45
7430	.15
7432	.30
7437	.35
7438	.35
7440	.25
7441	1.15
7442	.45
7443	.85
7444	.45
7445	.65
7446	.95
7447	.95
7448	.70
7450	.25
7451	.25
7453	.20
7454	.25
7460	.40
7470	.45
7472	.40

7473	.25
7474	.35
7475	.35
7476	.30
7480	.55
7481	.75
7483	.95
7485	.95
7486	.30
7489	1.35
7490	.55
7491	.95
7492	.95
7493	.40
7494	1.25
7495	.60
7496	.80
74100	1.85
74107	.35
74121	.35
74122	.55
74123	.55
74125	.45
74126	.35
74132	1.35
74141	1.00
74150	.85
74151	.75
74153	.95
74154	1.05
74156	.95
74157	.65
74161	.85
74163	.95
74164	.60
74165	1.50
74166	1.35
74175	.80

74176	1.25
74180	.85
74181	2.25
74182	.95
74190	1.75
74191	1.35
74192	1.65
74193	.85
74194	1.25
74195	.95
74196	1.25
74197	1.25
74198	2.35
74221	1.00
74367	.85
75108A	.35
75110	.35
75491	.50
75492	.50
74H00	.25
74H01	.25
74H04	.25
74H05	.25
74H08	.35
74H10	.35
74H11	.25
74H15	.30
74H20	.30
74H21	.25
74H22	.40
74H30	.25
74H40	.25
74H50	.25
74H51	.25
74H52	.15
74H53J	.25
74H55	.25

74H72	.55
74H101	.75
74H103	.75
74H106	.95
74L00	.35
74L02	.35
74L03	.30
74L04	.35
74L10	.35
74L20	.35
74L30	.45
74L47	1.95
74L51	.45
74L55	.65
74L72	.45
74L73	.40
74L74	.45
74L75	.55
74L93	.55
74L123	.55
74S00	.55
74S02	.55
74S03	.30
74S04	.35
74S05	.35
74S08	.35
74S10	.35
74S11	.35
74S20	.35
74S40	.25
74S50	.25
74S51	.45
74S64	.25
74S74	.40
74S112	.90
74S114	1.30

74S133	.45
74S140	.75
74S151	.35
74S153	.35
74S157	.80
74S158	.35
74S194	1.05
74S257 (8123)	.25
74LS00	.35
74LS01	.35
74LS02	.35
74LS04	.35
74LS05	.45
74LS08	.35
74LS09	.35
74LS10	.35
74LS11	.35
74LS20	.35
74LS21	.25
74LS22	.25
74LS32	.40
74LS37	.35
74LS40	.45
74LS42	1.10
74LS51	.50
74LS74	.65
74LS86	.65
74LS90	.95
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74LS107	.85
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LM320K5 (7905)	1.65
LM320K12	1.65
LM320T5	1.65
LM320T12	1.65
LM320T15	1.65
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8T13	1.50
8T23	1.50
8T24	2.00
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Circle 57 on inquiry card.

C Compiler Available for PDP-11, Planned for 8080

A compiler for the structured programming language C is now available for the PDP-11, and an 8080 version of the compiler is expected in early 1978. Because of its structured, table driven design, the compiler can be easily modified to produce object code for a new computer, thereby ensuring a consistent definition of the C language from one implementation to another. The compiler is said to generate code efficient enough to be used in real time system programming environments. A combined tutorial and reference manual affords easy access to the C language. The present compiler runs under the RSX operating system and is planned for other operating systems. It generates optimized code for each model of the PDP-11 from the 11/20 to the 11/70. The compiler is available on a lease basis for $11,575 from Yourdon Inc, 1133 Avenue of the Americas, New York NY 10036.■

Circle 585 on inquiry card.

Learn BASIC from Your Computer

This 6800 based package is designed to coach and prompt you to learn BASIC commands and programming techniques. Part I presents fundamental BASIC commands, while Parts II and III teach techniques of character string formatting, and reading and writing characters to cassette using BASIC and MIKBUG. Each part is priced at $13.95, with discounts for combinations of the three parts. An introductory sampler package is also offered for $6.95. The packages are supplied on cassette using the "Kansas City" recording standard, which can be read by the Southwest Technical Products AC-30 interface, and will run on a 12 K byte 6800 system. Contact Computerware Software Services, 830 First St, Encinitas CA 92024.■

Circle 586 on inquiry card.

New Business Forms for Small Computers

Computer forms designed for hobbyists and small systems users have been introduced by the Kenmor Company. Invoices, statements and other stock items made specifically for microcomputers are available in quantities of up to 5,000 sets. Company names or logos can be imprinted, and custom forms can also be supplied. The product line is aimed at small businesses, hobbyists, physicians, dentists, accountants, etc, who wish to update their billing and record systems.

Contact Kenmor Corporation, 675 McLean Av, Yonkers NY 10704, or call Roberta Fink at (914) 965-3006.■

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Management Problem Solving Library

Here's a library of programs for financial analysis complete with a two year updating service. Each program in the library is described in a user manual, and is said to be tested in a user environment prior to distribution. Library updates are issued quarterly and can be obtained for a nominal copying fee. The programs include present and future value problems, loan amortization problems, depreciation schedules for various depreciation methods, a complete real estate investment package, a cash budgeting program, and an elementary float analysis of check clearing. Versions are available for MITS Disk Extended BASIC and for North Star BASIC. The programs are available from Business Computer Systems, 216 Collier Dr, Springfield IL 62704, (217) 787-3448.■

Circle 588 on inquiry card.

Editor Lets You Create New Commands

ATE is an 8080 assembler, text editor and cassette operating system designed especially to run with the all purpose IO board from Morrow's Micro-Stuff. The editor borrows features such as text addressing and programming of loops and subroutines of editing commands from classical text editors like QED and TECO. The assembler can handle programs larger than memory, can produce object code listings in any number base, and allows editing of the object code. ATE fits in 4 K bytes and runs comfortably in 8 K bytes of programmable memory. Written by Gary Fitts, ATE is offered on a Kansas City standard cassette tape for $24.95 from Thinker Toys, 1201 10th St, Berkeley CA 94710, (415) 527-7548.■

Circle 589 on inquiry card.

Build Your Own Software System

The System Kit is a collection in book form of 8080 assembly language program modules and narrative text describing module functions and interfacing conventions (for parameter passing and register and memory use). It consists of building blocks for an operating system, a runtime linker and a miniloader which enables you to construct a custom system of your own design. The modules are grouped into a nucleus and four surrounding layers or "shells." Functions provided by the modules include clock, IO and console handling, memory and queue management, event processing and timeshared task scheduling, and similar operations. The System Kit is $50 from La Forge Enterprises, POB 410, Boalsburg PA 16827, (717) 564-2440.■

Circle 592 on inquiry card.

MIKADOS Adds Disassembler

The Mini Instant Keyboard Assembler, Debug and Operating System (MIKADOS) now includes a disassembler as well. The assembler translates assembly code directly to machine language as it is entered, resolving jumps and relative branches, and the disassembler produces a pseudo assembly code listing of a machine language program in memory. Other features include setting and clearing of breakpoints and ASCII and hexadecimal IO. The disassembler is offered to existing MIKADOS users for $5. The whole package fits in 3 K bytes of memory, comes with a 28 page user manual and a 90 day limited warranty against bugs, and costs $17.95 from Inpro Micro Systems, POB 7776, Van Nuys CA 91409.■

Circle 590 on inquiry card.

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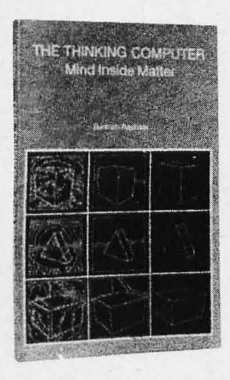
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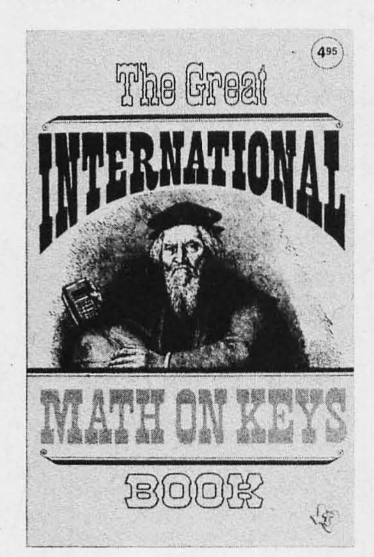
_____**The Thinking Computer: Mind Inside Matter** by Bertram Raphael. Artificial intelligence, or AI, is the branch of computer science concerned with making computers "smarter." It is a growing, vital field that is, unfortunately, the subject of much popular misunderstanding. **The Thinking Computer: Mind Inside Matter** is a lucid introduction to AI that does much to overcome this misunderstanding. With a minimum of technical jargon, this book discusses the capabilities of modern digital computers and how they are being used in contemporary AI research. It discusses the progress of AI, the goals, and the variety of current approaches to making the computer more intelligent. $6.95.



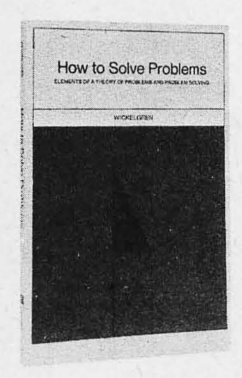


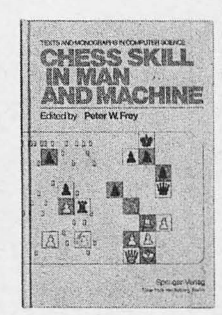
_____**Projects in Sight, Sound, & Sensation** by Mitchell Waite. Dedicated "to all space cowboys." Detailed theory and practice of seven fascinating amateur electronics projects, along with a complete and detailed appendix on how to make PC boards. The projects included in this book are: The Syntheshape, an art generator that can be used to generate innumerable complex and beautiful patterns on the screen of an oscilloscope. An electronic music box that will play over 3000 possible melodies when the lid is lifted. A way to control muscle tension explained in chapter 4. A muscle-wave biofeedback monitor can be used to achieve deep relaxation. The laser-light show transfers light into fascinating patterns in a darkened room. Other projects include a Kirlian camera, a digital ESP machine, and neonlight randomizer. $5.25.

_____**The Great International Math On Keys Book**, from Texas Instruments. Do you need a numerical algorithm for calculating exchange rates in a hotel on a foreign trip? Or figuring those mysterious "points" when facing the sanctimonious charisma of a banker at mortgage time? This book is a compendium of simple explanations and step by step procedures for accomplishing numerical solutions to numerous commonly encountered situations in daily life. Each entry is characterized by a statement of the problem, including the elements of theory required, and the keystrokes needed to solve the problem on an algebraic entry calculator. This is an invaluable sourcebook of information for the person who is inclined to manipulate numbers. $4.95.



_____**How to Solve Problems** by Wayne A Wickelgren. When confronted by a problem, many of us spend more time puzzling over **how** to solve it than in actually doing so. This book analyzes and systematizes the basic methods of solving mathematical problems. The methods are described in terms of a modern theory derived from research in computer simulation of thinking. Examples illustrating these methods include chess problems, logical puzzles, and railroad switching problems frequently encountered in science and engineering. Whether your interest in solving problems is professional, recreational, or both, you will find this a helpful book. $6.50 softcover.





_____**Chess Skill in Man and Machine** edited by Peter W Frey. This is a most fascinating book, concerning itself with the when, how, and why of computer chess. The when describes past ACM computer chess tournaments, with the details of more than a dozen games. The how consists of the basics of both human chess skill and computer chess theory. It includes a detailed description of the best computer chess program to date (Northwestern University's CHESS 4.5), an end game program called PEASANT, and of various search strategies and heuristic computer chess theory which should enable one to write his own chess program. The book ends with the why concerning the contributions, now and in the future, of computer chess to understanding artificial intelligence, human intelligence, and learning. The only difficulty for the hobbyist's computer chess program is the need for a large computer for the fast processing of search strategies and large core storage for the program and its results. $14.80 hardcover.

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Circle 10 on inquiry card.

BREAD BOARD JUMPER WIRE KIT



JK1 ....$10.00 / kit

Each kit contains 350 wires cut to 14 different lengths from 0.1" to 5.0'.

Each wire is stripped and the leads are bent 90° for easy insertion.

Wire length is classified by color coding.

All wire is solid tinned 22 gauge with PVC insulation.

The wires come packed in a convenient plastic box.

SOCKET JUMPERS

Mates with two rows of .025" sq. or dia. posts on patterns of .100" centers and shielded receptacles. Probe access holes in back. Choice of 6" or 18" length.

Part No.	No. of Contacts	Length	Price
924003-18R	26	18"	$ 5.38 ea.
924003-06R	26	6"	4.78 ea.
924005-18R	40	18"	8.27 ea.
924005-06R	40	6"	7.33 ea.
924006-18R	50	18"	10.31 ea.
924006-06R	50	6"	9.15 ea.

JUMPER HEADERS

Solder to PC boards for instant plug-in access via socket-connector jumpers. .025" sq. posts. Choice of straight or right angle.

Part No.	No. of Posts	Angle	Price
923863-R	26	straight	$1.28 ea.
923873-R	26	right angle	1.52 ea.
923865-R	40	straight	1.94 ea.
923875-R	40	right angle	2.30 ea.
923866-R	50	straight	2.36 ea.
923876-R	50	right angle	2.82 ea.

INTRA-CONNECTOR

Provides both straight and right angle functions. Mates with standard .10" x .10" dual row connectors (i.e. 3m, Ainsley, etc.) Permits quick testing of inaccessible lines.

Part No.: 922576-26 No. of contacts: 26 Price $6.90 ea.

INTRA-SWITCH

Permits instant line-by-line switching for diagnostic or QA testing. Switches actuated with pencil or probe tip. Mates with standard .10" x .10" dual-row connectors. Low profile design. Switch buttons recessed to eliminate accidental switching.

Part No.: IS-26 No. of contacts: 26 Price $13.80 ea.

CRYSTALS

THESE FREQUENCIES ONLY

Part #	Frequency	Case/Style	Price
CY1A	1.000 MHz	HC33/U	$5.95
CY2A	2.000 MHz	HC33/U	$5.95
CY2.01	2.010 MHz	HC33/U	$ .99
CY3A	4.000 MHz	HC18/U	$4.95
CY7A	5.000 MHz	HC18/U	$4.95
CY12A	10.000 MHz	HC18/U	$4.95
CY14A	14.31818 MHz	HC18U	$4.95
CY19A	18.000 MHz	HC18/U	$4.95
CY22A	20.000 MHz	HC18/U	$4.95
CY30B	32.000 MHz	HC18/U	$4.95

CONNECTORS

PRINTED CIRCUIT EDGE-CARD

.156 Spacing-Tin-Double Read-Out

Bifurcated Contacts — Fits .054 to .070 P.C. Cards

15/30	PINS (Solder Eyelet)	$1.95
18/36	PINS (Solder Eyelet)	$2.49
22/44	PINS (Solder Eyelet)	$2.95
50/100	PINS (Wire Wrap)	$6.95
50/100A (.100 Spacing)	PINS (Wire Wrap)	$6.95

25 PIN-D SUBMINATURE (RS232)

DB25P	PLUG	$3.25
DB25S	SOCKET	$4.95

SWITCHES

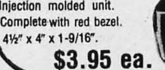
¼" mounting holes

Type	Part			1-9	10+
TOGGLE (sub-minature)	JMT121	SPDT	on-off-on	$1.95	$1.43
	JMT123	SPDT	on-none-on	1.65	1.21
	JMT221	DPDT	on-off-on	2.55	1.87
	JMT223	DPDT	on-none-on	2.15	1.58
TOGGLE (Printed Circuit)	MPC121	SPDT	on-off-on	$2.05	$1.53
	MPC123	SPDT	on-none-on	1.75	1.31
	MPC221	DPDT	on-off-on	2.65	1.97
	MPC223	DPDT	on-none-on	2.25	1.68
PUSH BUTTON	PB123	SPDT	maintained	1.95	1.47
	PB126	SPDT	momentary	1.95	1.47
PUSH BUTTON Minature	MS102	DPST	momentary open	.35	.30
	MS103	SPST	momentary closed	.35	.30
DIPSWITCH SPST	206-4	8 pin dip	4 switch	1.75	1.65
	206-7	14 pin dip	7 switch	1.95	1.85
	206-8	16 pin dip	8 switch	2.25	2.15

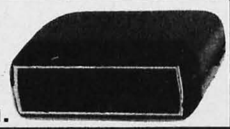
1/16 VECTOR BOARD

	0.1" Hole Spacing Part No.	P-Pattern L	W	Price 1-9	10 up
PHENOLIC	64P44 062XXXP	4.50	6.50	1.72	1.54
	169P44 062XXXP	4.50	17.00	3.69	3.32
EPOXY GLASS	64P44 062WE	4.50	6.50	2.07	1.86
	84P44 062WE	4.50	8.50	2.56	2.31
	169P44 062WE	4.50	17.00	5.04	4.53
	169P84 062WE	8.50	17.00	9.23	8.26
EPOXY GLASS COPPER CLAD	169P44 062WEC1	4.50	17.00	6.80	6.12

INSTRUMENT/ CLOCK CASE



Injection molded unit. Complete with red bezel. 4½" x 4" x 1-9/16".



$3.95 ea.

MICROPROCESSOR COMPONENTS

8080A	CPU	$16.00	CDP1802	CPU	$19.95
8212	8 Bit Input/Output	4.95	MC6800	8 Bit MPU	24.95
8214	Priority Interrupt Control	15.95	MC6820	Periph. Interface Adapter	15.00
8216	Bi-Directional Bus Driver	6.95	MC6810AP1	128 x 8 Static RAM	6.00
8224	Clock Generator/Driver	9.95	MC6830L8	1024 x 8 Bit ROM	15.00
8228	System Controller Bus Driver	10.95	Z80	CPU	29.95

CPU'S

8080A	Super 8008	16.00
2650	8 BIT MPU	26.50
P8085	CPU	29.95

SR'S

2504	1024 Dynamic	$ 3.95
2518	Hex 32 BIT	7.00
2519	Hex 40 BIT	4.00
2522	Dual 132 Bit SSR	2.95
2524	512 Dynamic	.99
2525	1024 Dynamic	3.00
2527	Dual 256 BIT	3.95
2529	Dual 512 BIT	4.00
2532	Quad 80 BIT	3.95
2533	1024 Static	5.95
3341	Fifo	6.95
74LS670	16 x 4 Reg	3.95

UART'S

AY-5-1013	30K Baud	$5.95

ROM'S

2513(2140)	Char. Gen.-upper case	$ 9.95
2513(3021)	Char. Gen.-lower case	9.95
2516	Char. Gen.	10.95
MM5230	2048 BIT (512 x 4 on 256 x 8)	1.95

RAM'S

1101	256 x 1	Static	$ 1.49
2101	256 x 4	Static	5.95
2102	1024 x 1	Static	1.75
2107/5280	4096 x 1	Dynamic	4.95
2111	256 x 4	Static	6.95
7489	16 x 4	Static	2.49
8101	256 x 4	Static	5.95
8111	256 x 4	Static	6.95
8599	16 x 4	Static	3.49
21L02/91L02	1024 x 1	Static	2.25
74200	256 x 1	Static	6.95
93421	256 x 1	Static	2.95
MM5262	2K x 1	Dynamic	3 for 1.00
UPD414(2104)	4K	Dynamic 16 Pin	5.95

PROMS

1702A	2048	Famos	$ 9.95
5203	2048	Famos	14.95
82S23	32 x 8	Open C	5.00
82S123	32 x 8	Tristate	5.00
74S287	1024	Static	7.95
3601	256 x 4	Fast	3.95
2708	8K	Eprom	19.95
2716	16K	Eprom	34.95
6301-1	1024	Tri-State Bipolar	3.49
6330-1	256	Open Collector Bipolar	2.95

SPECIAL REQUESTED ITEMS

FCM3817	$5.00	11C90	19.95	7205	19.95	9368	3.95
AY-3-8500-1	9.95	4N33	3.95	ICM7045	24.95	LD110/111	25.00/set
AY-5-9100	17.50	8T20	7.50	ICM7207	7.50	95H90	11.95
AY-5-9200	14.95	8T97	2.00	ICM7208	22.00	MC3061P	3.50
AY-5-9500	4.95	HD0165	7.95	ICM7209	7.50	MC4016 (74416)	7.50
AY-5-2376	14.95	MCM6571	13.50	MK50240	17.50	MC1408L7	8.95
9374	1.95	MCM6574	13.50	DS0026CH	3.75	MC1408L8	9.95
82S115	25.00	MCM6575	13.50	TIL308	10.50	74C922	9.95

CLOCK CHIPS

MM5309	$9.95
MM5311	4.95
MM5312	4.95
MM5314	4.95
MM5316	6.95
MM5318	9.95
MM5369	2.95
MM5841	9.95
CT7001	5.95

PARATRONICS

Featured on February's Front Cover of Popular Electronics

Logic Analyzer Kit Model 100A

$229.00/kit

Model 100A Model 10

- Analyzes any type of digital system
- Checks data rates in excess of 8 million words per second
- Trouble shoot TTL, CMOS, DTL, RTL, Schottky and MOS families
- Displays 16 logic states up to 8 digits wide
- See ones and zeros displayed on your CRT, octal or hexadecimal format
- Tests circuits under actual operating conditions
- Easy to assemble — comes with step-by-step construction manual which includes 80 pages on logic analyzer operation.

(Model 100A Manual - $4.95)

- Some applications are:
  - — Troubleshooting microprocessor address, instruction, and data flow
  - — Examine contents of ROMS
  - — Tracing operation of control logic
  - — Checking counter and shift register operation
  - — Monitoring I/O sequences
  - — Verifying proper system operations during testing

PARATRONICS TRIGGER EXPANDER - Model 10

Adds 16 additional bits. Provides digital delay and qualification of input clock and 24-bit trigger word. — Connects direct to Model 100A for integrated unit).

Model 10 Kit - $229.00
Baseplate — $9.95
Model 10 Manual — $4.95

B+K PRECISION

3½-Digit Portable DMM

- Overload Protected
- .3" high LED Display
- Battery or AC operation
- Auto Zeroing
- 1mv, 1Va, 0.1 ohm resolution
- Overange reading
- 10 meg input impendence
- DC Accuracy 1% typical

Ranges: DC Voltage ±0-1000V/
AC Voltage: 0-1000V
Freq. Response: 50-400 HZ
DC/AC Current: 0-100mA
Resistance: 0-10 meg ohm
Size: 6.4" x 4.4" x 2"

Model 2800 $99.95

Comes with test leads, operating manual and spare fuse.

Accessories:

AC Adapter BC-28	$9.00
Rechargeable Batteries BP-26	20.00
Carrying Case LC-28	7.50

CSC

100 MHz 8-Digit Counter

- 20 Hz-100 MHz Range
- .6" LED Display
- Crystal-controlled timebase
- Fully Automatic
- Portable — completely self-contained
- Size — 1.75" x 7.38" x 5.63"
- Four power souces, i.e. batteries, 110 or 220V with charger 12V with auto lighter adapter and external 7.2-10V power supply

MAX-100 $134.95



ACCESSORIES FOR MAX 100:

Mobile Charger Eliminator use power from car battery — **Model 100 — CLA $3.95**

Charger/Eliminator use 110 V AC — **Model 100 — CAI $9.95**

CONTINENTAL SPECIALTIES

PROTO BOARD 6

$15.95
(6" long X 4" wide)

Other CS Proto Boards

PB100 - 4.5" x 6"	$ 19.95
PB101 - 5.8" x 4.5"	29.95
PB102 - 7" x 4.5"	39.95
PB103 - 9" x 6"	59.95
PB104 - 9.5" x 8"	79.95
PB203 - 9.75 x 6½ x 2¾	80.00
PB203A - 9.75 x 6½ x 2¾ (includes power supply)	129.95

PROTO CLIPS

14 PIN	$4.50
16 PIN	4.75
24 PIN	8.50
40 PIN	13.75

DESIGN MATES

DM1 - Circuit Designer $69.95
DM2 - Function Generator $74.95
DM3 - RC Bridge $74.95

LOGIC MONITOR for DTL, HTL, TTL or CMOS Devices **$84.95**

CSC QT PROTO STRIPS

QT type	#holes	price
QT-59S	590	12.50
QT-59B	bus strip	2.50
QT-47S	470	10.00
QT-47B	bus strip	2.25
QT-35S	350	8.50
QT-35B	bus strip	2.00
QT-18S	180	4.75
QT-12S	120	3.75
QT-8S	80	3.25
QT-7S	70	3.00

Experimentor 300	$ 9.95
Experimentor 600	$10.95

$5.00 Minimum Order — U.S. Funds Only
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Spec Sheets - 25¢ — Send 35¢ Stamp for 1978 Catalog
Dealer Information Available

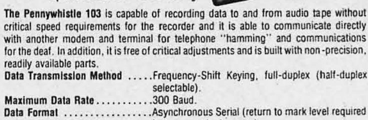
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James ELECTRONICS

1978 CATALOG NOW AVAILABLE

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Advertised Prices Good Thru March

The Incredible "Pennywhistle 103"



$129.95 Kit Only

The Pennywhistle 103 is capable of recording data to and from audio tape without critical speed requirements for the recorder and it is able to communicate directly with another modem and terminal for telephone "hamming" and communications for the deaf. In addition, it is free of critical adjustments and is built with non-precision, readily available parts.

Data Transmission Method .....Frequency-Shift Keying, full-duplex (half-duplex selectable).
Maximum Data Rate ....300 Baud.
Data Format ....Asynchronous Serial (return to mark level required between each character).
Receive Channel Frequencies ...2025 Hz for space; 2225 Hz for mark.
Transmit Channel Frequencies ..Switch selectable: Low (normal) = 1070 space, 1270 mark; High = 025 space, 2225 mark.
Receive Sensitivity ....−46 dbm accoustically coupled.
Transmit Level ....−15 dbm nominal. Adjustable from −6 dbm to −20 dbm.
Receive Frequency Tolerance ...Frequency reference automatically adjusts to allow for operation between 1800 Hz and 2400 Hz.
Digital Data Interface ....EIA RS-232C or 20 mA current loop (receiver is optoisolated and non-polar).
Power Requirements ....120 VAC, single phase, 10 Watts.
Physical ....All components mount on a single 5" by 9" printed circuit board. All components included.

Requires a VOM, Audio Oscillator, Frequency Counter and/or Oscilloscope to align.

NEW! BULB-ENERGY SAVER



Bulb lasts 3 or more times longer. Fits Standard Socket 6 watts to 200 watts

BES-1 1-9 $1.50 ea. 10+ 1.25 ea.

BULB-ENERGY SAVERS used for years by major industrial users — now available for home or office use. Bulb Savers can cut electrical bills by as much as 3%.

BULB-SAVERS lengthens light life by:

1. Acting as an electrical "shock absorber", turns the bulb on slowly, eliminating the "thermal shock". Bulb life increases 300 percent.
2. Banishes Current "Surges". Cushions line voltage surges when other loads cut power line.
3. Reduces Energy Consumption

DIGITAL STOPWATCH

- Bright 6 Digit LED Display
- Times to 59 minutes 59.59 seconds
- Crystal Controlled Time Base
- Three Stopwatches in One
  Times Single Event — Split & Taylor
- Size 4.5" x 2.15" x .90" (4½ ounces)
- Uses 3 Penlite Cells.



Kit — $39.95
Assembled — $49.95
Heavy Duty Carry Case $5.95

Stop Watch Chip Only (7205) $19.95

iMC 3½DIGIT DPM KIT



- New Bipolar Unit
- Auto Zeroing
- .5" LED
- Auto Polarity
- Low Power
- Single IC Unit

Model KB500 DPM Kit $49.00
Model 311D-5C-5V Power Kit $17.50

JE700 CLOCK



12 or 24 Hour

115 VAC

The JE700 is a low cost digital clock, but is a very high quality unit. The unit features a simulated walnut case with dimensions of 6" x 2½" x 1". It utilizes a MAN72 high brightness readout, and the MM5314 clock chip.

KIT ONLY **$16.95**

HEXADECIMAL ENCODER 19-KEY PAD



- 1 - 0
- ABCDEF
- Shift Key
- 2 Optional Keys

$10.95 each

New 63 KEY KEYBOARD

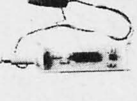
$29.95 IN STOCK



This keyboard features 63 unencoded SPST keys, unattached to any kind of P.C.B. A very solid molded plastic 13" x 4" base suits most applications.

HD0165	Encoder Chip (encodes 16 Keys)	$7.95 ea.
AY-5-2376	Encoder Chip (encodes 88 Keys)	$14.95 ea.

JE803 PROBE

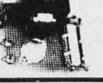


The Logic Probe is a unit which is for the most part indespensible in trouble shooting logic families TTL, DTL, RTL, CMOS. It derives the power it needs to operate directly off of the circuit under test, drawing a scant 10 mA max. It uses a MAN3 readout to indicate any of the following states by these symbols (H) - 1 (LOW) - o (PULSE) - P. The Probe can detect high frequency pulses to 45 MHz. It can't be used at MOS levels or circuit damage will result.

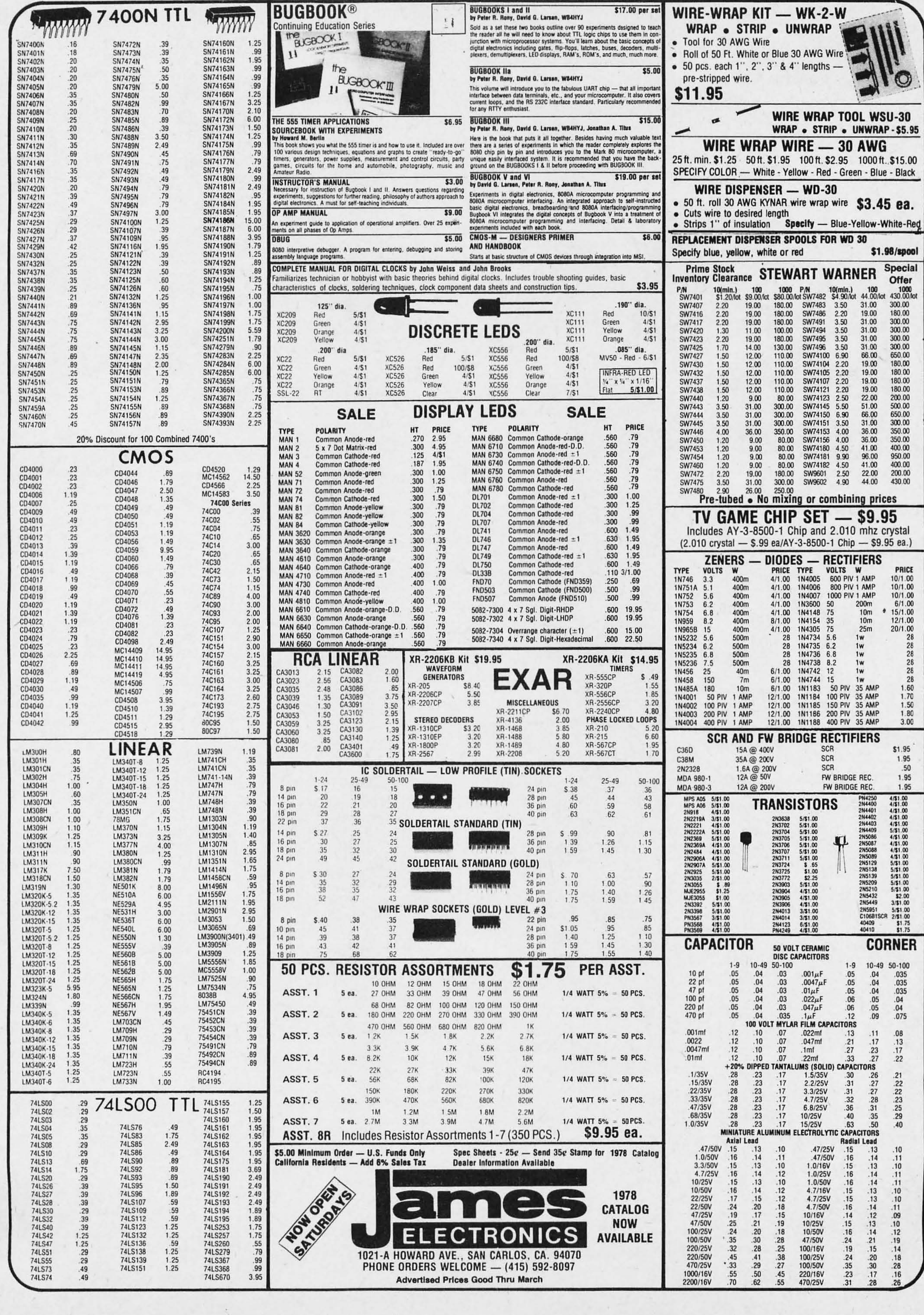
$9.95 Per Kit

printed circuit board

T²L 5V 1A Supply



This is a standard TTL power supply using the well known LM309K regulator IC to provide a solid 1 AMP of current at 5 volts. We try to make things easy for you by providing everything you need in one package, including the hardware for only **$9.95 Per Kit**



Circle 60 on inquiry card.

New Catalog of Circuit Design Aids



The 24 page *Complete Bugworks* catalog describes more than 155 circuit design and educational products. The contents include solderless sockets, breadboards and accessories, plug in functional modules called "outboards," designer "breadboxes" which include power supplies, controls and displays, and the MMD-1 Mini-Micro Designer microcomputer development system. The hardware is supported by a set of 16 texts including the popular Bugbook series of combined texts and lab manuals. The catalog is available from E & L Instruments Inc, 61 First St, Derby CT 06418, (203) 735-8774.■

Circle 616 on inquiry card.

Game Playing with BASIC

This book includes over 60 computer games and puzzles such as three-dimensional Tic Tac Toe, Nim, Roulette, Go-Moku, and many others. The author describes the rules of each game and includes illustrative flowcharts and diagrams. The last chapter contains 26 games and puzzles for reader solution. *Game Playing with BASIC,* written by Donald D Spencer, is available paperbound for $6.95 from Hayden Book Company Inc, 50 Essex St, Rochelle Park NJ 07662, (201) 843-0550.■

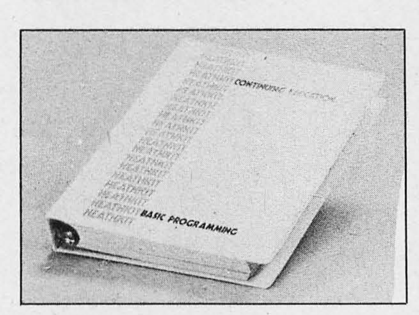
Circle 617 on inquiry card.

Care and Feeding of Floppy Disks

This free brochure offers suggestions for the safe handling and storage of floppy disks. The publisher manufacturers a storage cabinet and indexing system for keeping track of a library of floppies, priced at $59.95 for a limited time. The brochure is available from Advance Access Group Inc, 10526 W Cermak, Westchester IL 60153, (312) 562-5210.■

Circle 618 on inquiry card.

Learn BASIC with This Self Instruction Course



The EC-1100 course combines programmed instruction text with practical demonstration programs and practice problems to teach BASIC language formats, commands, statements and procedures. The course goes beyond conventional BASIC texts to give the student an introduction to the creative and problem solving aspects of programming in BASIC. The EC-1100 course is keyed to the Heath computer systems, but it could be a useful supplement for other computers using BASIC. The course is priced at $29.95 and is further described in a free catalog available from Heath Company, Dept 350-450, Benton Harbor MI 49022.■

Circle 621 on inquiry card.

Computer Store Survey Rates Manufacturers

An opinion survey of the nation's computer stores rates the top 37 personal computer manufacturers on 17 performance parameters such as delivery, packaging, warranty, pricing and reliability. Prepared from questionnaires and telephone interviews covering 450 stores, the survey also deals with business problems, trends, and market characteristics as seen by store managers. For more information including prices, contact Image Resource, 717 Lakefield Rd, Suite B, Westlake Village CA 91361, (805) 495-6277.■

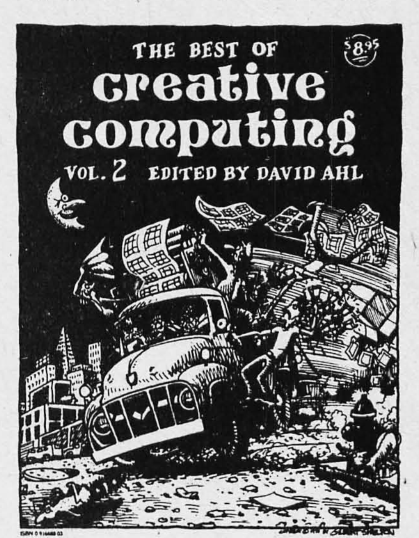
Circle 622 on inquiry card.

How to Fix Your Own Cassette Recorder

The *Workbench Guide to Tape Recorder Servicing* shows you how to fix problems with portable cassette recorders, open reel tape decks and 8 track cartridge players. It covers topics such as how to disassemble any machine in short order, how to make sense out of manufacturers' specifications sheets, and how to pinpoint problems in tape transport mechanisms. Written by G Howard Poteet, the book is $10.95 from Parker Publishing Company Inc, West Nyack NY 10994.■

Circle 623 on inquiry card.

Highlights from Creative Computing



This book contains a collection of articles, fiction, foolishness, puzzles, programs, computer games and reviews from the Volume 2 (1976) issues of *Creative Computing* magazine. During this period, home computers just began coming on the scene. This volume reflects the transition from minis and timesharing terminals to the new microsystems, although the diversity of the contents guarantees there will be something for just about everyone.

15 new computer games are described with complete listings and sample runs for each; 67 pages are devoted to puzzles, problems, programs, and things to do with your computer or terminal. Frederik Pohl drops in for a visit along with ten other imaginative storytellers. The staggering diversity of this book makes it an ideal point from which to jump into the amazing world of recreational or educational computing.

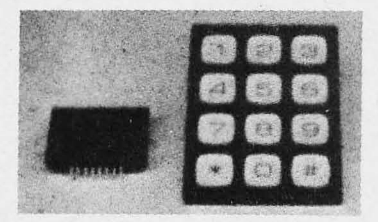
The Best of Creative Computing – Volume 2 is available for $9.95 postpaid from Creative Computing, Attn: Pamela, POB 789-M, Morristown NJ 07960.■

Circle 619 on inquiry card.

Book of MUMPS

This new book describes applications of MUMPS, the Massachusetts General Hospital Utility Multiprogramming System. MUMPS is a powerful interpretive language featuring text editing and searching capabilities, a hierarchical file system, and a shared data base with multiple users, which has been used for many medical applications. The 48 page *Book of MUMPS* lists 230 MUMPS application programs and 197 institutions which are using MUMPS. Information is also included on the MUMPS Users' Group (MUG) and its application library, MUMPS vendors and other MUMPS publications. The book is $2 from the MUMPS Users' Group, 700 S Euclid Av, St Louis MO 63110, (314) 454-3364.■

Circle 620 on inquiry card.



TOUCH TONE ENCODER KIT

Simplicity itself to complete. No other parts required, no crystal required. The back of the touch pad has etched & drilled PC board and you solder the encoder chip to it. Add your own small speaker & 9 volt battery and you are done. A touch of the pad produces the proper tone signal from the speaker. We furnish schematic and instructions.

SP-149-B $12.95

WIRE WRAP WIRE

TEFZEL blue #30 Reg. price $13.28/100 ft. Our price 100 ft $2.00; 500 ft $7.50.

MULTI COLORED SPECTRA WIRE

Footage			10'	50'	100'
8	Cond.	#24	$2.50	9.00	15.00
12	"	22	3.00	11.00	18.00
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Great savings as these are about 1/4 book prices. All fresh & new.

TOUCHTONE ENCODER CHIP

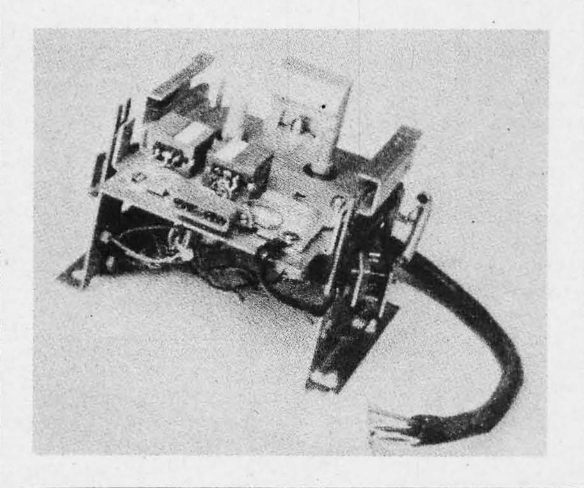
Compatible with Bell system, no crystal required. Ideal for repeaters & w/specs. $6.00

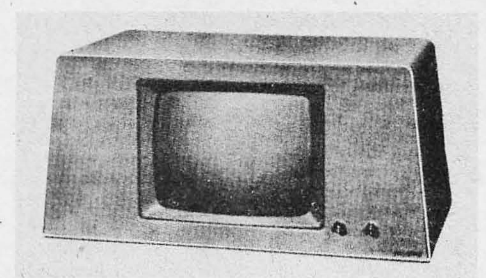
LAMBDA POWER SUPPLIES

LM-D-12-OVP 12 volts DC 10 amp $60, LV-EE 5-OVP 5 VDC 74 Amp $75.00

VIATRON CASSETTE DECKS

The computer cassette deck alone $35. Set of Control boards for above $40.



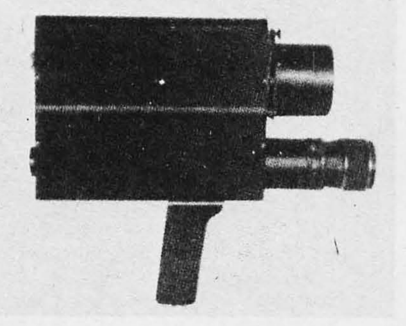


VIDEO DISPLAY from Viatron systems. Accepts composite video signals. 9 inch transistorized CCTV black & white CRT monitor. Ready to go, checked out. 115 volt AC 60 cycle. With circuit diagram.

$75.00

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Custom made, complete with light source & viewer in one piece. Comes with carrying strap. Ready to operate with 6 volt lantern battery. Guaranteed by the manufacturer. See in total darkness. Great for scientists, viewing nocturnal animals & birds, criminal investigation . . . observe without being observed, and a ball for just plain snooping!!!! Sorry to say but no shipments to Calif. (lens may vary slightly from pic)

SPL-21 $199.00

Meshna

Please add shipping cost on above. Minimum order $10

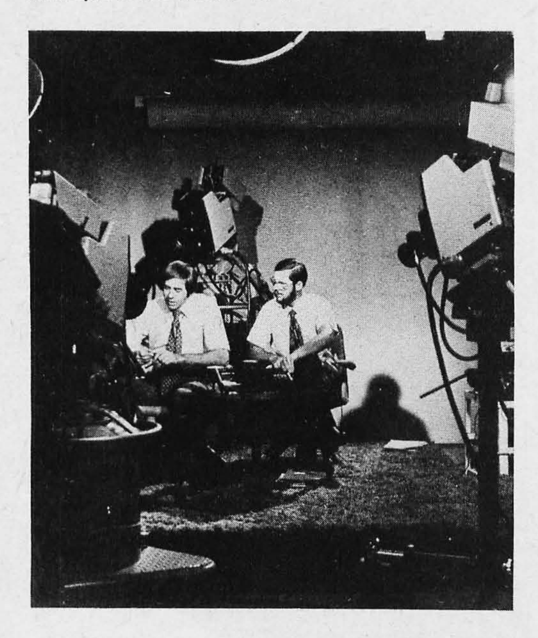
FREE CATALOG NOW READY # SP-10

P.O. Box 62, E. Lynn, Massachusetts 01904

Circle 66 on inquiry card.

What's New?

Microprocessor Course on TV



An instructional course in microprocessors for industry, designed around the Micro-68 training computer, is now available in the form of 30 half hour color video cassette sessions. The course was developed by Electronic Product Associates Inc in conjunction with Colorado State University. Course materials include the textbook *Understanding Microprocessors*, the *6800 Programming Manual* and *System Design Reference Manual*, the *Micro-68 Lab Manual* and *Micro-68 User's Manual*, and a course study guide. The cassette package may be purchased for $7060 including one Micro-68 computer trainer and one set of documentation, or it may be leased for as little as $875 and $140 for the computer trainer. Additional computer trainers are available at the discounted price of $533. A 30 minute preview tape may be rented for a week for $50. The course is available from the university or from Electronic Product Associates Inc, 1157 Vega St, San Diego CA 92110, (714) 276-8911.■

Circle 593 on inquiry card.

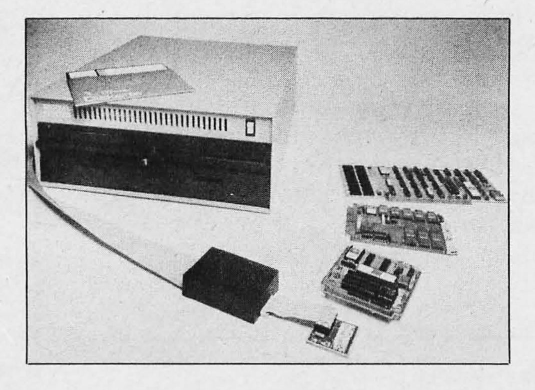
Gang Write Your EROMs With This Programmer



The Model 16 gang programmer is capable of programming nearly one million bytes of erasable read only memory per hour. The unit simultaneously programs 16 EROMs; includes a built in calibration mode; provides ROM continuity tests which detect faults in memory, socket connections, and programmer electronics; automatically pretests the programmer voltages; and computes checksums to ensure the integrity of the programmed information. RS232C serial IO at selectable data rates is included, and an interactive alphanumeric display simplifies operation. The Model 16 measures 8 by 13 by 23 inches (20.32 by 33.02 by 58.42 cm), weighs 38 pounds and costs $4800 from Data I/O Corp, POB 308, Issaquah WA 98027, (206) 455-3990.■

Circle 594 on inquiry card.

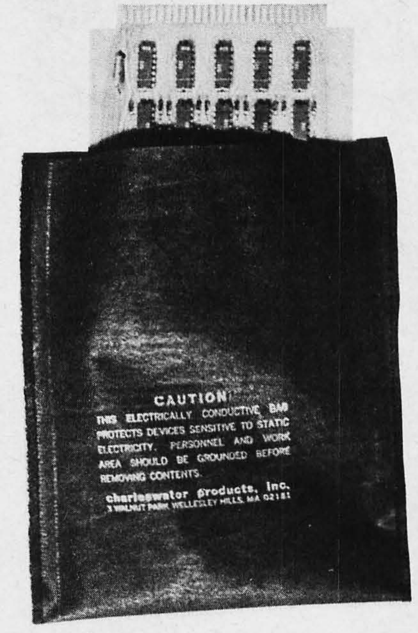
Universal Emulator Features Flexible Assembler



This Z-80 based development system combines a flexible assembler with a memory emulation module to provide a development system for any microprocessor. The assembler can handle arbitrary instruction mnemonics including multibyte op codes like those of the Z-80. The assembler's symbol table can be set up with the mnemonics for an 8080, 6800, F8, etc, and programs for the selected microprocessor can then be assembled. The system comes with a Z-80 processor, 32 K bytes of memory, 4 K bytes of emulator memory, and a dual drive floppy disk. An operating system, editor, assembler and utilities are provided. Also included are up to four buffered connectors which are designed to plug into 2708 EROM sockets in the target system. Priced at $5995, the emulator is available from M & E Associates, 10439 N Stelling Rd, Cupertino CA 95014.■

Circle 595 on inquiry card.

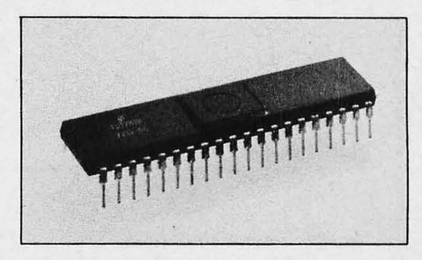
Protect Circuit Boards with These Conductive Bags



CP302 Statfree Conductive Bags are made of electrically conductive nonwoven nylon material to protect MOS, CMOS and other sensitive electronic components from static electricity. The bags come in sizes from 5 by 8 inches (12.7 by 20.32 cm) to 10 by 18 inches (25.4 by 45.72 cm) and have a tensile strength in excess of 7500 pounds per square inch. The manufacturer will imprint a company name and model number on the bags. Prices start at $21.50 per 100 bags, from Charleswater Products Inc, 3 Walnut Park, Wellesley MA 02181, (617) 237-5942.■

Circle 596 on inquiry card.

Dual Density Floppy Controller Chip



The FD1781 floppy disk controller and formatter chip is completely compatible with TTL and will accommodate the interface systems of most disk manufacturers. Its features include automatic track seek with verification, selectable track to track stepping, head settling and engage times, double buffering of data, and an 8 bit bidirectional bus interface for communication with the computer. It provides data, data strobe and address mark IO for reading and writing data and can handle a variety of encoding and formatting methods. The FD1781 is available from Western Digital Corp, 3128 Red Hill Av, Newport Beach CA 92663, (714) 557-3550.■

Circle 597 on inquiry card.

ASCII KEYBOARD . . .

With direct addressable interface to S-100 or other bus

OR . . . COMPLETE VIDEO TERMINAL

Can all be housed in attractive enclosure below



FEATURES

- 49 keys plus space bar, shift, and shift lock.
- Minimum 10 additional keys for control, lower case, system reset, etc. (some illuminated).
- Outputs TTL compatible.
- Keyboard interface is tri-state; address decoding capability eliminates need for external I/O board.
- Serial board (w/RS232 interface) or complete video terminal fits into cabinet under keyboard.
- Single supply voltage (plus 12V or plus 5V), less than 150 mils drain.
- Excellent commercial quality (manufactured by Cherry).
- Attractive, sturdy cabinet in simulated walnut and black vinyl.

Through a fortunate purchase of new and used surplus keyboards, coupled with some imaginative design, we are able to offer professional quality I/O capabilities for any minicomputer system or for use as a stand-alone remote terminal. Simply add a video monitor (or converted TV set) and save at least 50% by buying one of the **keyboard-video interface** combinations described below.

KEYBOARD ONLY . . . . $ 44.95
Above configured to serve as addressable input port with cable 54.95
Above, as direct plug-in to the S-100 bus 69.95
Keyboard with serial board incl. RS232 interface . . . 84.95

Keyboard with complete video terminal (adapted version of ESAT-100), 16x32 format — 2 pages, with serial interface from 300 to 9600 baud (conversion kit to 16x64 will be available), full cursor control, kit 199.95
Above, built and tested 249.95

With 16x64 video board (adapted version of Xitex's SCT-100) upper and lower case, 128 characters, with both serial ASCII and BAUDOT capabilities, full X-Y cursor control, kit 249.00
Above, built and tested 299.95

With 24 x 80 video board (adapted version of Dynabyte 57), upper and lower case, addressable cursor and block mode editing, built and tested 399.95
Above units are supplied as stand-alone units. For direct interface to system bus . . . . ADD $ 10.00
When interfaced to an S-100 bus, video board can be in main cabinet for service convenience. Please specify use.

Reconditioned 12-inch 14 MHz monitors . . . . $ 109.95
New monitors and modems available.

Keyboards without interface or case — available at greatly reduced prices.

Above keyboards are used, in excellent condition, and are guaranteed for 90 days. Limited quantity of new units available — ADD $30.00 to any of above prices.

Add $2.00 for handling, shipping, and insurance.

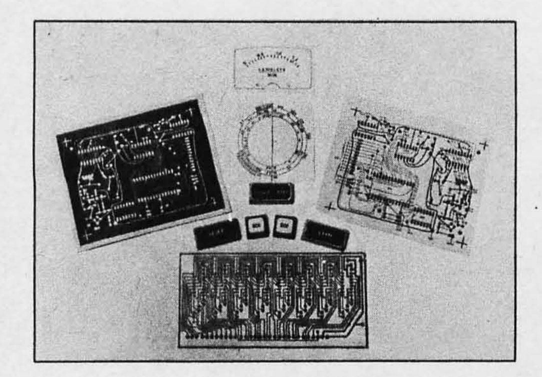
Send for free 64-page catalog of other values.

MiniMicroMart, Inc. 1618 James Street, Syracuse, N.Y. 13203 (315) 422-4467

Circle 74 on inquiry card.

What's New?

Make Printed Circuit Boards with This Film



This film can be used without cameras or chemicals to make printed circuit boards, component placement decals, front panel faces and similar patterns directly from a printed page as in a magazine construction article. A six step process is used to complete a transfer in less than 15 minutes. Prices for the film range from $5.49 for a small package of six 4 by 6 inch (10.16 by 15.24 cm) pieces to $7.95 for a large package of three 9 by 12 inch (22.86 by 30.48 cm) pieces, from Printed Circuit Products Co, POB 4034, Helena MT 59601.■

Circle 598 on inquiry card.

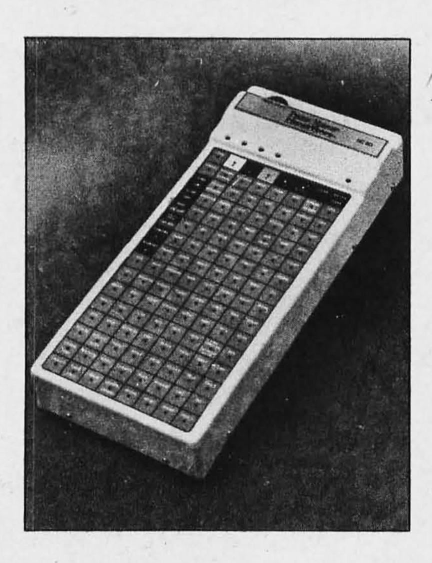
Wrap Your Own with These Rolls



Industrial quality AWG30 wire wrapping wire is now available in convenient 50 foot rolls on 1 5/8 inch diameter spools. The wire comes in four colors, red, white, blue and yellow, from OK Machine and Tool Corp, 3455 Conner St, Bronx NY 10475, (212) 944-6600.■

Circle 599 on inquiry card.

Hand Held Speech Synthesizer



The Phonic Mirror HandiVoice hand held speech synthesizer enables vocally impaired individuals to talk. The device produces phonemes rather than words and hence can articulate virtually any English word through some combination of phonemes. Two models of the synthesizer are available: the HC 120 which features a numeric keyboard and liquid crystal display, similar to a pocket calculator, with vocabulary selections made via three digit codes, designed for individuals with lower motor skills and higher cognitive skills, and the HC 110, which features a touch sensitive display board with 128 stations representing words, pictures or symbols, designed for individuals with lower cognitive skills and higher motor skills. The synthesizer electronics were originally developed for industrial use by Votrax, a division of Federal Screw Works. Sold only after referral by a professional speech pathologist or therapist, special education teacher or physician, the Phonic Mirror HandiVoice is manufactured by HC Electronics Inc, a division of American Hospital Supply Corp, One American Plz, Evanston IL 60201, (312) 866-4237.■

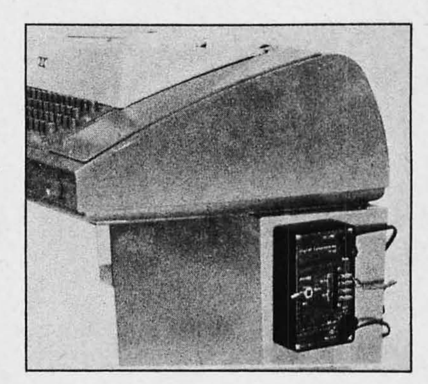
Circle 600 on inquiry card.

Radio Shack Offers the 8080A

That old stalwart, the 8080A microprocessor chip, can now be purchased in Radio Shack stores around the country as stock number 276-2510 (most likely in a bubble pack). The 100% prime chip is priced at $17.95. This fact like nothing else symbolizes the microprocessor's penetration into the everyday world of consumer electronics.■

Circle 601 on inquiry card.

XOFF Junk Characters Forever



This smart motor control allows a Teletype to print and punch paper tape without producing junk characters during an on-off cycle. The Model TR20 is an external motor control with a six character storage capability that provides a 0.6 second delay for the Teletype motor to speed up and print. The unit mounts by magnet to the Teletype pedestal. It connects directly to the motor through a fuse plug device and does not interfere with the options panel. The Model TR20 features a bypass switch to permit standard keyboard operation. An adjustable timer provides up to a 20 second turnoff delay. The unit is 6 by 3.5 by 3 inches (15.2 by 8.9 by 7.6 cm), weighs one pound and operates on 110 V current.

The Model TR20 is guaranteed for two years and sells for $175 from Digital Laboratories, 600 Pleasant St, Watertown MA 02172, (617) 924-1680.■

Circle 602 on inquiry card.

New TV Interface RF Modulator Handles Color and Sound

The Pixie-Plexer Model PXP-4500 is a special RF modulator for multiplexing and interfacing color and luminance video signals plus audio to any TV set through the antenna terminals. Features include a 3.5 MHz color subcarrier oscillator and a 4.5 MHz audio subcarrier complete with varactor diode modulator for FM sound insertion. The PXP-4500 may be operated as a simple monochrome character display or a multiplexer plus modulator for color difference inputs and audio subcarrier signals. The device is built from a single integrated circuit on a 1.5 by 3 inch (3.81 by 7.62 cm) board with printed circuit RF coils. A single 15 V power supply (optionally −12 V and 5 V) at 50 mA is required. The kit comes complete with assembly instructions and a data sheet on the integrated circuit. The PXP-4500 is $24.50 from computer stores nationwide or direct from the manufacturer, ATV Research, 13th and Broadway, Dakota City NB 68731, (402) 987-3771.■

Circle 603 on inquiry card.

POLY PAKS

COMPUTER PERIPHERAL & PARTS WORKSHOP

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POLY PAKS SPECIAL

BUY $15 WORTH Take **10%** DISCOUNT

BUY $100 WORTH Take **25%** DISCOUNT

FROM THIS AD ONLY

"RED" LED READOUTS!

as low as **20¢ each**

Cat. No.	Size	Description	Sale
□ 3S1890	.127"	MAN-3**	5 for $1.00
□ 3S1503	.19	MAN-4*	2 for $1.19
□ 3S1273	.27	MAN-1*	$1.00
□ 3S3093	.33	MAN-72 equal*	$1.19
□ 3S3161	.33	MAN-74 equal**	$1.19
□ 3S3512	.35	FND359**	$1.00
□ 3S2949	.5	FND500*	$1.50
□ 3S2950	.5	FND507*	$1.50
□ 3S3483	.5	727-Dual**	$2.50
□ 3S2485	.5	727-Dual*	$2.50
□ 3S2256	.6	747*	$1.95

*Common Anode **Common Cathode

HEXADECIMAL MICROPROCESSOR AND CONTROL KEYBOARD KIT! □ 29^95

Address microprocessors, control computer operated equipment. 2 key rollover. Has 20 keys, 16 encoded, 4 external to be assigned by user. Output 4 bit binary. Also, an EXCLUSIVE FEATURE...4 leds display the binary output. TTL/CMOS compatible, requires +5, -12VDC. Complete kit! Nothing else to buy! With instructions.

Wt. 2 lbs.

- 4 bit binary/hexadecimal output plus strobe!
- New! Improved design! Saves you time!
- Keyboard pre-assembled onto PC board!

20 Key

Cat. No. 3S5009 Hexadecimal Kit $29.95
Cat. No. 3S5010 Hexadecimal Wired $34.95

DISCRETE LED'S 6 for $1.19

Order in multiples of 6 of each type!

□ JUMBO .34" h
□ MEDIUM .24"
□ MICRO .21" (TO-18)

Cat. No.	Description	Similar to
□ 3S2135	Jumbo Red	MV5053
□ 3S1944	Jumbo Yellow	XC556Y
□ 3S2138	Jumbo Green	XC556G
□ 3S2785	Medium Red	XC22
□ 3S2788	Medium Green	XC22G
□ 3S2137	Micro Red	XC209
□ 3S1948	Micro Yellow	XC209Y
□ 3S2140	Micro Green	XC290G

$49.95 NEW KEYBOARD & ENCODER KIT

• Uses Encoder MOS ROM • 7 "LED" test feature

Cat. No. 3S5001 Kit $49.95
Cat. No. 3S5002 Wired $59.95

Outputs standard 7 bit ASCII; interfaces with most data systems. Keyboard pre-assembled onto PC board, 2 key rollover. Electronic shift lock and carriage return. 4 modes: Normal, control, shift, shift/control. Additional functions can be assigned by user. +5, -12VDC, 200 ma. Negative or positive logic, jumper selectable. Exlcusive test feature...7 LED's display the ASCII code. Complete kit, nothing else to buy! Size: 13" x 5 1/2 x 1 1/4". 3 lbs.

- Uses MOS Encoder ROM!
- 7 LED Test Feature!
- 64 key keyboard!
- Encodes 128 ASCII Characters
- Interfaces with ALTAIR, IMSAI, and more!

MICROPROCESSORS! MEMORIES! SUPPORT!

Order by Cat. No. 3S3459 and type

Type	Description	Sale
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□ 8080A	8 bit CPU, 2 usec	14.95
□ Z80A	8 bit CPU	34.95
□ 8008	CPU	9.95
□ 1101	256 x 1 stat. RAM	.69
□ 1103	1K Dyn RAM	1.29
□ 1702A	256 x 8 EPROM	5.95
□ 2102-L1	1K x 1 Lo-power RAM	1.69
□ 2111	256 x 4 Stat. RAM	5.95
□ 2708	8K EPROM	19.95
□ MK4116	16K Dyn RAM	32.00
□ MK4200P11	4K x 1 Dyn RAM, 350nsec	3.95
□ MM5202	2K PROM	6.95
□ MM5203	2K EPROM	8.95
□ MM5260	1K Dyn RAM	.99
□ MM5262	2K x 1 Dyn RAM	.99
□ 8212	8 bit I/O port	3.95
□ 8216	Bi-direct bus driver	3.95
□ 8224	Clock Gen	4.95
□ 8228	System cont.	9.95
□ 8251	Communication int	11.50
□ 8255	Periph inter	11.95

COMPUTER GRADE CAPACITORS

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Mfd	WVCD	Sale
□ 8,000	50	$2.75
□ 13,000	40	2.25
□ 14,000	50	2.75
□ 15,000	12	1.50
□ 22,000	75	3.95
□ 24,000	30	2.50
□ 44,000	30	3.95

FULL WAVE BRIDGE RECTIFIERS!

PIV	2 AMP (#3S1346)	6 AMP (#3S2456)	10 AMP (#3S2447)	25 AMP (#3S2273)
□ 50	$ .59	$ .88	$1.05	$1.20
□ 100	.65	.99	1.15	1.25
□ 200	.69	1.19	1.29	1.95
□ 400	.89	1.40	1.79	2.95
□ 600	.99	1.69	1.95	3.95
□ 800	1.19	1.95	2.25	4.95
□ 1000	1.25	2.25	2.50	5.50

Orer by Cat. No. Amperage and Voltage

Low Power ICs

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Type	Sale	Type	Sale
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□ 74LS02	.32	□ 74LS138	1.24
□ 74LS04	.35	□ 74LS139	1.24
□ 74LS08	.32	□ 74LS151	1.25
□ 74LS10	.32	□ 74LS153	1.25
□ 74LS11	.32	□ 74LS155	1.25
□ 74LS13	.64	□ 74LS160	1.47
□ 74LS20	.32	□ 74LS161	1.47
□ 74LS21	.32	□ 74LS162	1.47
□ 74LS22	.32	□ 74LS163	1.47
□ 74LS27	.39	□ 74LS168	1.68
□ 74LS30	.32	□ 74LS169	1.68
□ 74LS32	.39	□ 74LS173	1.68
□ 74LS37	.45	□ 74LS174	1.05
□ 74LS38	.45	□ 74LS190	1.77
□ 74LS42	1.19	□ 74LS191	1.75
□ 74LS47	.99	□ 74LS192	1.75
□ 74LS74	.49	□ 74LS193	1.75
□ 74LS90	.89	□ 74LS195	1.25
□ 74LS92	.89	□ 74LS197	1.25
□ 74LS93	.89	□ 74LS257	1.35
□ 74LS109	.58	□ 74LS266	.54
□ 74LS112	.58	□ 74LS366	.66
□ 74LS113	.58	□ 74LS368	.69
□ 74LS114	.49	□ 74LS390	2.95

C-MOS

Order By Cat. No. 3S2320 & Type No.

Type	Sale	Type	Sale
□ CD4000	$.29	□ CD4022	1.19
□ CD4001	.29	□ CD4023	.29
□ CD4002	.29	□ CD4024	.79
□ CD4006	1.19	□ CD4025	.34
□ CD4007	.29	□ CD4027	.69
□ CD4008	.79	□ CD4028	.89
□ CD4009	.59	□ CD4029	1.19
□ CD4010	.59	□ CD4030	.49
□ CD4011	.29	□ CD4033	1.60
□ CD4012	.29	□ CD4035	.99
□ CD4013	.69	□ CD4040	1.19
□ CD4015	1.19	□ CD4041	1.25
□ CD4016	.49	□ CD4042	.88
□ CD4017	1.19	□ CD4046	1.79
□ CD4018	1.19	□ CD4049	.49
□ CD4019	.49	□ CD4066	.79
□ CD4020	.99	□ CD4071	.29
□ CD4021	1.29		

TTL'S

Type	Sale	Type	Sale
□ SN7400	$0.14	□ SN7472	.26
□ SN7401	.14	□ SN7473	.31
□ SN7402	.17	□ SN7474	.31
□ SN7403	.14	□ SN7475	.48
□ SN7404	.17	□ SN7476	.39
□ SN7405	.18	□ SN7483	.69
□ SN7406	.19	□ SN7485	.88
□ SN7407	.24	□ SN7486	.29
□ SN7408	.18	□ SN7490	.69
□ SN7410	.14	□ SN7492	.45
□ SN7411	.19	□ SN7493	.45
□ SN7413	.39	□ SN74107	.29
□ SN7414	.61	□ SN74121	.31
□ SN7417	.24	□ SN74123	.49
□ SN7420	.14	□ SN74125	.39
□ SN7427	.26	□ SN74132	.83
□ SN7430	.14	□ SN74145	.89
□ SN7432	.24	□ SN74151	.63
□ SN7437	.24	□ SN74153	.63
□ SN7440	.14	□ SN74154	.99
□ SN7441	.79	□ SN74157	.64
□ SN7442	.49	□ SN74161	.87
□ SN7445	.69	□ SN74164	.95
□ SN7446	.79	□ SN74174	.93
□ SN7447	.79	□ SN74175	.88
□ SN7448	.75	□ SN74181	1.95
□ SN7450	.14	□ SN74190	1.15
□ SN7451	.14	□ SN74191	.99
□ SN7470	.28	□ SN74192	.83
		□ SN74193	.83
		□ SN74195	.75
		□ SN74251	1.39

SPECTRA-TWIST RIBBON CABLE

• Twisted pairs of brightly colored cable! 24AWG

□ Cat. No. 3S3680 48 cond. 2 ft. $1.98
□ Cat. No. 3S4081 32 cond. 2 ft. $1.98

RIBBON CABLE AT THIN PRICES

- Ultra-flat! • 28 AWG!
- Single color! Indexed!

Cond.	Sale
□ 20	8 ft. $1.98
□ 26	6 ft. $1.98
□ 34	5 ft. $1.98
□ 40	4 ft. $1.98
□ 50	3 ft. $1.98

Order by Cat. No. 3S3939 and conductors

SILICON POWER STUD RECTIFIERS!

Order by Cat. No. Amperage and voltage.

PIV	12 AMP (#3S727)	50 AMP (#3S727)	250 AMP (#3S685)
□ 50	$ .29	$ .75	$4.95
□ 100	.36	1.10	6.50
□ 200	.45	1.35	7.50
□ 400	.61	1.75	8.50
□ 600	.79	2.25	10.50
□ 800	.90	2.75	11.50

POLY PAKS "CHIPS" AWAY IC AND CRYSTAL PRICES!

Order by Cat No. 3S4048 and Type No!

Type	Description	Sale
□ ICM7205	Stopwatch	$14.95
□ AY3-8500-1	6 TV Games	9.95
□ MM5330	4½ Digit DVM	4.95
□ 8038C	Volt Control Osc.	4.95
□ KR2376-139	BCD Encoder Rom	6.95
□ KR2376-ST	ASCII Encoder Rom	14.95
□ 11C90DC	650MHz Prescaler	14.95
□ 95H90DC	350MHz Prescaler	8.88
□ MC14410	Touch Tone Chip	9.95
□ MK2002P	Char Gen. (sim 2513)	3.95
□ 7207A/7208	Freq Counter pair	24.95
□ ICM7107	3½ Digit DVM/DMM	12.50
□ MM5316	Alarm Clock	2.95
□ MM5369	60 Hz Timebase IC	1.95
□ 3.579MHz	Timebase Xtal	1.95
□ 1.00MHz	Touchtone Xtal	5.95
□ 3.2768MHz	Stopwatch Xtal	4.95

SOLAR ENERGY DISCS

- All Cells .5V!
- High efficiency!
- Gang for higher voltages and amps!

As low as **$3.95**

Cat. No.	Size	Mils	Sale
□ 3S5046	2"	500ma	$3.95
□ 3S3862	3"	1000ma	8.88
□ 3S3788	3½"	1200ma	12.50
□ 3S5057	4"	1500ma	15.95

LINEARS

Type	Sale	Type	Sale
□ LM301H, V	$.25	□ LM379N	4.95
□ LM307H, V, N	.25	□ LM380N	1.19
□ LM308H, V	.79	□ LM381N	1.19
□ LM309K	1.19	□ LM555V	.44
□ LM311H, V	.79	□ LM558V	.69
□ LM320T-5V	1.19	□ LM565N	.65
□ LM320T-15V	1.19	□ LM567V	1.40
□ LM320K-12V	1.19	□ LM703H	.39
□ LM320K-15V	1.19	□ LM709H, N	.22
□ LM340T-5V	1.19	□ LM710N	.29
□ LM340T-12V	1.19	□ LM723N	.42
□ LM340T-15V	1.19	□ LM741H, V, N	.29
□ LM340K-5V	1.19	□ LM747H, N	.59
□ LM340K-12V	1.19	□ LM1458V	.69
□ LM340K-15V	1.19	□ LM1800N	1.49
□ LM322N	1.19	□ LM3900N	.35
□ LM324N	.99	□ LM39009V	1.19
□ LM339N	1.09	□ LM75491	.69
□ LM377N	1.50	□ LM75492	.75
		□ PA263	1.50

SPECTROL "SKINNY-TRIMS"

Ohms
□ 50
□ 100
□ 500
□ 1K □ 10K
□ 2K □ 20K
□ 5K □ 50K

3/8" square, screwdriver shaft, 2% tol, 1/4 watt. Cermet. PC leads. Order by Cat. No. and value.

Your Choice **2 for $1**

□ Cat. No. 3S3863 25 turn upright, type 64
□ Cat. No. 3S3866 single turn, flat, type 63

10 AMP POWER TAB SCR'S, TRIACS, QUADRACS!

Order by Cat. No. and Voltage

	Cat. No.
SCR'S	3S1730
TRIACS	3S1448
QUADRACS	3S1590

PIV	SALE
□ 50	$.55
□ 100	.69
□ 200	.88
□ 400	1.19
□ 600	1.59

DIP SWITCHES

	Cat. No.	Switches	Sale
□	3S3668	2	$.77
□	3S3669	3	.88
□	3S3021	4	.99
□	3S3670	5	1.19
□	3S3671	6	1.29
□	3S2677	7	1.79

MOTHERBOARD EDGE CONNECTOR

□ **$3.95**

106 pins (53 each side). Use with IMSAI & ALTAIR! 0.125" pin ctrs, goldplated 5/8" wire wrap leads. Open ends, fit wide PC boards. 8 ozs. Cat. No. 3S3987



1N4000 EPOXY RECTIFIERS

- Miniature!
- 1.5 Amp!

Order by Cat. No. and Type No.

	Cat. No.	Type No.	PIV	Sale
□	3S2377	1N4001	50	10 for $.65
□	3S2378	1N4002	100	10 for .75
□	3S2379	1N4003	200	10 for .85
□	3S2380	1N4004	400	10 for .99
□	3S2381	1N4005	600	10 for 1.29
□	3S2382	1N4006	800	10 for 1.39

EECO 10-POSITION BCD THUMBWHEEL SWITCH

1-2-4-8 BCD encoding! Positions labeled 0-7, F, L. (F coded for 8, L coded for 9). White numerals on a black background. Eeco 800 series. 1¼ x 1¼ x ½". Cat. No. 3S3846

3 for $4. □ **$1.49**

COMPUTER GRAPHICS "JOYSTICK"

2 for $8. □ **$4.50**

- Four 100K pots!
- Chrome handle and knob!

Wt. 10 oz. Cat. No. 3S3808A

GIANT SALE! MICRO-MINI TOGGLE SWITCHES

*Center off

- Top Quality!
- 3A, 125VAC contacts or better!
- Complete with mounting hardware!

Cat. No.	Contacts	Sale
□ 3S3936	SPST	$1.19
□ 3S4036	SPDT	1.29
□ 3S5085	SPDT*	1.39
□ 3S4037	DPDT	1.45
□ 3S5087	4PDT*	1.95

TRANSFORMER SALE

LOOK!

• 110VAC Primaries

	Cat. No.	Output V.	Amps	Misc.	Sale Each
□	3S3399	6.3V	500ma	Metal encased	$1.98
□	3S3814	6.3V	1A	Open frame	$2.49
□	3S3412	12V	300ma	Open frame	$1.95
□	3S4029	12V	1A	Open frame	$2.49
□	3S4028	12V	1A	Metal encased	$2.95
□	3S3323	24VCT	300ma	Open frame	$1.95
□	3S3937	24V	1A	Open frame	$1.95
□	3S2773	48VCT	2A	Metal encased	$2.95
□	3S3875	110V	300ma	Isolation	$1.19

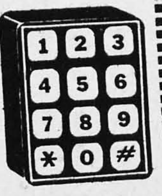
"MICRO-TONE" AUTOPATCH ENCODER KIT

- Emergency!
- Family!
- Friends!
- Complete in its own mini-cabinet!

28^88 □.

Only 2 1/8 x 1 5/8 x 1/2", small enough to mount in a mike! Snap action bubble keys contact. Features output level control, xtal controlled digitally synthesized tones, on-chip oscillator. Requires 4.5 to 5.5 VDC. Complete kit! Nothing else to buy! Wt. 12 oz.

Cat. No. 3S4086 kit $28.88
Cat. No. 3S4087 wired $34.95





HANDY COMPUTER MULTITESTER

• 1000 ohms per volt

1% precision, movements diode protected against burnout. Measures DC volts 0-15-150-1000; AC volts 0-15-150-1000; DC current 0-150ma; resistance X1000. Sensitivity 1000 ohms/volt AC-DC. Uses penlite cell, not included. Size 2⅜ x 3½ x 1⅜". Wt. 5 ozs. Cat. No. 3S3921

IC SOCKETS

as low as **17¢ ea.**

• Low profile, solder tail.

Cat. No.	Description	Sale
□ 3S2123	8 pin minidip	$ .17
□ 3S1308	14 pin dip	.19
□ 3S1309	16 pin dip	.22
□ 3S3378	18 pin dip	.25

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Terms: Add postage Rated: net 30
Phone: Wakefield, Mass. (617) 245-3829
Retail: 16-18 Del Carmine St., Wakefield.

MINIMUM ORDER — $6.00

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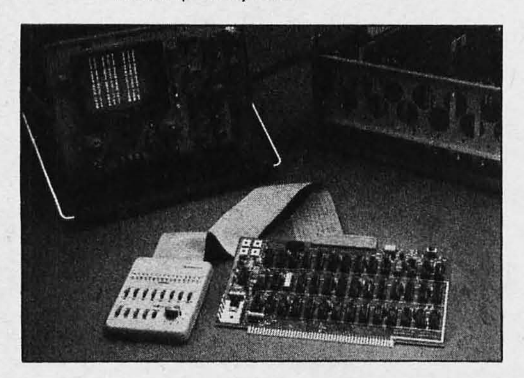
C.O.D.'s MAY BE PHONED

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Circle 96 on inquiry card.

What's New?

Logic Analyzer Plugs Into Altair (S-100) Bus

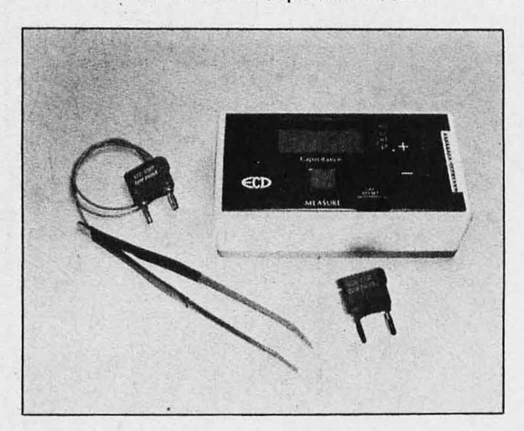


The Model 150 "Bus Grabber" logic analyzer electrically and mechanically interfaces to the Altair (S-100) bus, monitoring 56 key bus signals without the need for the numerous and unwieldy input probes associated with nondedicated instruments. Included in the 56 signals are the address and data bus and the microprocessor status, interrupts and control signals. In addition to the 56 dedicated signals, eight user defined signals interface to the plug-in board through an optional flat ribbon assembly. The associated probe tips can be used with ball clips, wire wrap pins or integrated circuit clips on any kind of equipment. Triggering of up to 24 bits, display formatting and operational modes of the logic analyzer are controlled from a small hand held pod connected to the plug in board through a ribbon cable. Data "grabbed" from the Altair (S-100) bus or other signals are displayed as ones and zeroes on an ordinary oscilloscope connected through the horizontal, vertical and (optionally) blanking inputs. Signals can be captured and stored in the analyzer's 16 bit wide by 16 word deep data memory and displayed on the oscilloscope as a series of eight truth tables, each 8 bits wide by 16 words deep. Data can also be formatted into hexadecimal and octal binary groupings. Other features include automatic clock qualification and clock polarity selection, and choice of pre or post trigger data acquisition.

The Model 150 logic analyzer is available in kit form for $369 or assembled for $449, with an optional external 8 bit probe set for $9.95, from Paratronics Inc, 800 Charcot Av, San Jose CA 95131, (408) 263-2252.■

Circle 624 on inquiry card.

New Probe for Capacitance Meter



This chip probe for ECD Corp C-Meter expands the capability of the hand held 3-1/2 digit battery operated capacitance meter to function as a unique inexpensive portable measuring tool for chip capacitors. Costing $39, the chip probe consists of a pair of tweezers connected to a double banana plug by a small diameter coaxial cable. The probe plugs directly into the C-Meter's standard banana jack input terminal. The cable capacitance is cancelled by the C-Meter "offset adjustment" located on the front panel. Connection to the chip capacitor terminals is made simply by permitting the tweezer tines to touch the capacitor terminal ends. The probe is designed for use with chips whose terminal spacing is from 0.02 inches to 0.300 inches and with values greater than 0.1 picofarads. The ECD C-Meter, which features autoranging, measures from 0.1 picofarads to 200,000 microfarads and automatically indicates the capacitor's value on its large LCD display. The C-Meter is $289 from ECD Corp, 196 Broadway, Cambridge MA 02139.■

Circle 625 on inquiry card.

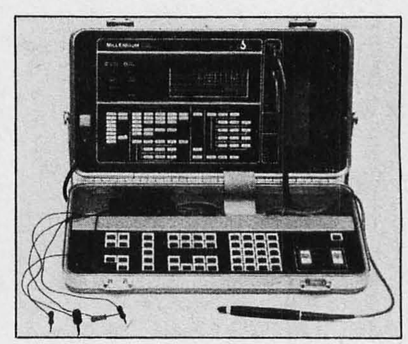
In Circuit Debugging for COSMAC Based Systems



The CDP18S030 COSMAC Micromonitor is a hardware and software debugging tool which can be attached by means of a single cable connection to the system under test. Controlled by its own microprocessor, the device uses the 1802 processor, power supply, clock, memory and other components of the system under test to run a user program. The Micromonitor provides an extensive set of debugging facilities, including 43 commands to examine and modify registers and memory, set breakpoints based on flag lines, interrupts and memory requests, and run the program in full speed, single instruction or single machine cycle modes. Self-contained in an attache case, the Micromonitor includes a built in keyboard, display and status indicator lights. It is priced at $1600 in single quantities and is described in the PD18 brochure from RCA Solid State Division, POB 3200, Somerville NJ 08876.■

Circle 627 on inquiry card.

Millennium Arrives in Logic Analyzers



This diagnostic tool is designed to allow technicians of limited skill to isolate component faults in microprocessor based products. The Microsystem Analyzer combines signature analysis with a circuit emulation to ease troubleshooting of complex products. An umbilical cord is plugged into the microprocessor socket of the system under test, and bit patterns are generated which cause predictable bit streams to appear at various points in the system. The analyzer is designed for universal use, by incorporating one processor for operator interaction functions and a second processor for functions related to the system under test. Operator interaction is carried out through a function oriented keyboard and a 20 character alphanumeric display. Test programs may be keyed into the unit's programmable memory or stored in read only memory chips which can be plugged into the unit. The unit's mother board and card cage provide room for optional expansion boards. Options include a real time trace feature and an RS232 connection for remote use. The Microsystem Analyzer is priced at $2475, while the signature analysis probe option is $495, from Millennium Systems Inc, 19020 Pruneridge Av, Cupertino CA 95014, (408) 966-9109.■

Circle 626 on inquiry card.



Circle 97 on inquiry card.

Classified Ads

FOR SALE: 4 K programmable memory printed circuit boards for 2102 type memories (and others). Brand new commercially made boards with plated thru holes and gold fingers. I have about six extras to sell at 2 for $15, with diagram and edge connector, postpaid, money order please. Steve Kelley, 9506 Peach St, Oakland CA 94603.

16 BIT FREAKS: Interested in saving $50 on the new Texas Instruments Tm 990/100m-1 16 bit microcomputer module? It is factory assembled and has programmable memory, Rom monitor, serial and parallel interface, and fully buffered expansion bus. See photo on page 218 in September BYTE. For more information contact J E Brancheau, POB 67, Trenton MI 48183.

FOR SALE: IBM 5100 with APL, 48 K, serial IO, 5103 printer, current IBM service contract. Was $18,450 new. Asking $16,950. Peter Goltra, Rt 2, Box 31, Middleburg VA 22117, (703) 687-6976.

FOR SALE: IMSAI 8080 with 4 K IMSAI programmable memory, 22 slot motherboard, IBM Selectric IO writer, and REMEX high speed paper tape reader. $950. Jeffrey Borish, 1669 Whitwood Ln, Apt 3, Campbell CA 95008, (408) 379-8278 evenings.

SOFTWARE: Exchange. North Star Disc Media Let's swap. Send SASE to HBR, POB AF, Woodbridge CT 06525.

FOR SALE: HP-97 Calculator, $525, with box of paper rolls and all fresh magnetic cards. Absolutely clean, 100% functional, still in warranty. Brewer Pedin, 4307 Wyncliff Dr, Richmond VA 23235, (804) 272-6291.

FOR SALE: Microcomputer, Mostek F8, documentation, regulated (5 V, 2 A; 12 V, 1 A) supply, RS232 to 20 mA circuit. In top condition. Make an offer. Paul Snigier, 360 Pleasant St, Raynham MA 02767, (617) 822-1329 evenings.

WANTED: BYTE #2, October 1975. Will trade mint condition #1, September 1975, or #13, September 1976, or pay cash. D Kenney, 82 Fifth Av, Westbury NY 11590, (516) 334-7362.

FOR SALE: All issues of BYTE from September 1975 to August 1977, except for December 1976. Best offer within one month after ad's appearance. Stephen Douglass, 348 Edgemeer Pl, Oberlin OH 44074, (216) 775-2492.

I NEED HELP! I need schematics, electrical specs and operating or technical manual for a Friden 7102 Communications Terminal. I will buy the manuals or pay for copies. My terminal has two boards missing. Has anyone any extras? M Dean Klingler, POB 930, Rialto CA 92376.

WILL SWAP: Pentax Spotmatic single lens reflex camera with built-in automatic metering, Pentax f: 1.4 50 mm normal lens plus Sun 38-90 mm zoom lens for Altair 8800, IMSAI 8080, SwTPC 6800, or similar minicomputer. Roger T Stevens, 5301 Rawlings Rd NE, Albuquerque NM 87111.

Readers who have equipment, software or other items to buy, sell or swap should send in a clearly typed notice to that effect. To be considered for publication, an advertisement should be clearly noncommercial, typed double spaced on plain white paper, and include complete name and address information. These notices are free of charge and will be printed one time only on a space available basis. Insertions should be limited to 100 words or less. Notices can be accepted from individuals or bona fide computer users clubs only. We can engage in no correspondence on these and your confirmation of placement is appearance in an issue of BYTE.

Please note that it may take three or four months for an ad to appear in the magazine.■

FOR SALE: One fully assembled and fully operational SOL-PC with SOLOS operating system. All documentation and software (BASIC, GAMEPAC I) included, $600. Contact R Coates, 3508 SE Washington St, Portland OR 97214.

WANTED: Univac 0769-06 printer service manual containing exploded mechanical diagrams with part numbers, schematic of -06 drive and interface card, timing information, etc. Will pay reasonable price or copy charge. Also want commercial cabinet or enclosure for this machine, or exceptional homemade one. Anyone out there in BYTE land have any of the above, or know of any? Leroy Lawler, 3101 Justin Way, Concord CA 94520.

PROM PROGRAMMING: From binary or hexadecimal paper tape: 1702A ($4), 2708 ($8). From hexadecimal or octal listing: 1702A ($5), 2708 ($16). You supply the PROM. I have a few 1702A PROMS available at $6 each. Quantity discounts on programming. 48 hour turnaround. H S Corbin, 11704 Ibsen Dr, Rockville MD 20852, (301) 881-7571.

FOR SALE: Ohio Scientific, OSI Challenger, with 12 K fast programmable memory, 440B video board, 430B cassette interface, 20 mil TTY port. With extras: memory board, CPU board, IO board, 480 backplane, ASCII keyboard, full manual set with all MOS manuals. Software includes: 8 K BASIC on cassette and paper tape (by Microsoft), 4 K miniBASIC on cassette, OSI extended monitor, plus programs in BASIC. Much more. Take all for $1200 or call for separate pricing and more details. Just plug in TV or monitor and go. Will ship UPS in USA. Mark Gilger, 3306 S Maple, Rapid City SD 57701, (605) 342-4190.

WANTED: Information on IBM Model 11-C electric typewriter. Also information on Clary Model DE600 computer. Steven D Swift, 15302 5th NE, Seattle WA 98155.

1802: Instruction set summary for the 1802 COSMAC, newly arranged in a compact, logical, typeset, 1 sheet format. Provides great aid for program writing and debugging, excellent introduction to what the 1802 can do (quite a lot!). Available for $1 plus SASE, from Seth McEvoy, Box 268, E Lansing MI 48823. Uses RCA's instructions, operations and mnemonics.

FOR SALE: SONEX touch-tone computer terminal, $350. J Herrault, 645 Bush, Apt 307, San Francisco CA, (415) 391-9439.

FOR SALE: Litton, ABS 1210 decimal computer, drum memory 375 (10 digit) words. System includes processor, drum, console and parallel IO ASR 33. Price $1000 or offer. Roy, 8224 Calumet Av, Munster IN 46321, (219) 836-1222.

FOR SALE: Two 8 K Solid State Music memory boards, 500 ns, static, plus spare ICs, all for $380. Color video recorder plus video camera and zoom lens, plus extra video cassettes; all for $400. Larry Wright, Box 7576, Menlo Park CA 94025, (415) 854-5678.

WANTED: 36 contact double sided PC board extenders (total 72 contacts). Contact centers 0.2 inch. Maximum card width 7-1/2 inches, preferable 6 inches long. Also, Winchester Electronics MRE9 9 pin rectangular plug connector or equivalent. Both for Burroughs Agent Set. Gilbert R Bossé, Box 185, Riviere au Renard, Quebec CANADA GOE 2A0, (418) 269-3256.

FOR SALE: BYTE issues 1 thru 12, best offer. SwTPC CT-1024 TVT, complete with memory board and power supply, modified for 64 characters and scrolling, all ICs in sockets, full documentation, $150 postpaid. A P Stumpf, Box 1603, Litchfield Park AZ 85340.

FOR SALE: Must sell due to move into rotten old house. Two Teletypes 33ASR (paper tape reader and punch with keyboard/printer). Both have been used on IMSAI system. One has a Digital Equipment Corp (DEC) PDP-8 interface installed. Regular TTY $675, PDP-8 interface TTY $725, plus shipping one high-speed paper tape reader Digitronics Model 2540. Can be used on two S-100 parallel ports. Has an interface for a Data General Nova microcomputer. $900 plus shipping, one Lear Siegler ADM-3 CRT terminal. Used regularly with IMSAI system. Upper and lower case option included. $775 plus shipping. One Anderson Jacobson AJ841 Selectronic terminal. Used for hardcopy with IMSAI system. Uses EBCD encoding on keyboard and Selectric printer. $950 plus shipping. Call or write: Ed Reich, 805 N Cleveland St, Arlington VA 22201, (703) 243-3131 evenings.

FOR SALE: Diablo Hytype II printer. Never used. 8 1/2 inch pin feed platen, cover and bottom feed. Interface to your 8080 or 6800. $1399 without power supply, $1799 with power supply. Roger Gersonde, 3950 N 54 St, Milwaukee WI 53216, (414) 462-1582.

FOR SALE: MCS 6502 resident assembler/text editor (ASSM/TED). Syntax very similar to MOS Technology. Produces relocatable object code on tape or executable object in memory. Relocating loader program also provided. 17 commands and 16 pseudo ops. User specifies memory area for text file and symbol table, up to 10 characters per label, 18 error codes, supports two tape decks, CRT and keyboard and printer. Shipped preconfigured for TIM based systems but information is provided to modify for others. Resides in less than 4 K (excluding source file and symbol table) (0200-1200, 0400-1400, 1000-2000, 2000-3000, please specify). Hexadecimal listing and operator's manual, $25. C W Moser, 3239 Linda Dr, Winston-Salem NC 27106.

WANTED: Speech Lab kit or assembled board and documentation or manuals by themselves. State condition and price. H S Corbin, 11704 Ibsen Dr, Rockville MD 20852, (301) 881-7571.

WANTED: Information concerning the conversion of an SwTPC CT-1024 terminal to 64 characters per line. Contact John Burns, 25th Floor, 350 Park Av, New York 10022.

WANTED: Plotter, drum or bed, any size, any condition. Send complete description along with price and/or trade requirements to Mark Sproul, 1368 Noah Rd, North Brunswick NJ 08902.

FOR SALE: Hewlett-Packard Dymec Data Acquisition System. Model 2515A high speed digital scanner; Model 2911A guarded cross bar scanner; Model 2911B crossbar scanner control; Model 2546A magnetic tape coupler; and Cook Model 150, 7 track tape recorder. Above system, complete with manuals and rack, $300. Hewlett-Packard Model 5275A Time Interval Counter, $70. Will deliver within 100 miles or you pay shipping. Donald Dorson, Gardner Rd, West Kingston RI 02892, (401) 294-2190.

IS THERE LIFE ON THIS PLANET? What happened to Life (as we know it)? Life is the cellular automata developed by John Conway and described by Martin Gardner in Scientific American (I don't have the dates). Life is great fun, an intellectual pastime, and high powered math all rolled into one. The possibilities with Conway's game are enough to keep you busy for a while, and, if this should pale, make up your own! Conway chose the rules for his game; you can make your own. When you do this, you have a completely new universe. In Life, the cells that determine the next generation are adjacent to the cell in question. They don't have to be. Life is symmetrical. Try it some other way. Life is two-state. Make your own with four states, each represented by a different character (or color). Make an automata in which the next generation is based on the preceding two generations, instead of one. Each change produces a new universe to be explored. Two needs exist: people to create universes, and people to explore. I will serve as a Life clearinghouse, and if interest is shown, create a flyer. If interested, or you have any information on Conway's game or others, let me know. Contact me, Rick Coates, 3508 SE Washington St, Portland OR 97214.



S.D. SALES CO. AN EMPIRE IND. CO.

P.O. BOX 28810B DALLAS, TEXAS 75228

S.D. SALES NEW EXPANDABLE EPROM BOARD

16K or 32K EPROM $49.95 w/out EPROM

Allows you to use either 2708's for 16K of Eprom or 2716's for 32K of Eprom.

KIT FEATURES:

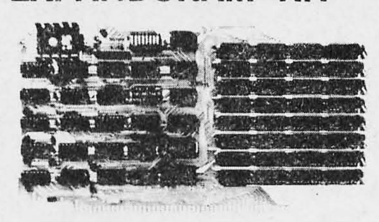
1. All address lines & data lines buffered.
2. Quality plated through P.C. Board, including solder mask and silk screen.
3. Selectable wait states.
4. On board regulation provided.
5. All sockets provided w/board.

WE CAN SUPPLY 450ns 2708's AT $11.95 WHEN PURCHASED WITH BOARD.

32K FOR $475 EXPANDORAM KIT 24K FOR $367.00

MEMORY CAPACITY
MEMORY ADDRESSING
MEMORY WRITE PROTECTION

8K, 16K, 24K, 32K using Mostek MK4115 with 8K boundaries and protection. Utilizes DIP switches. PC board comes with sockets for 32K operation. Orders now being accepted. Allow 6 to 8 weeks for delivery.



INTERFACE CAPABILITY
Control, data and address inputs utilizes low power Schottky devices.

POWER REQUIREMENTS
+8VDC 400MA DC
+18VDC 400MA DC
—18VDC 30MA DC

on board regulation is provided. On board (invisible) refresh is provided with no wait states or cycle stealing required.

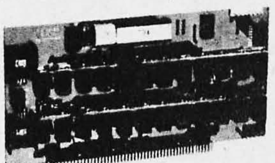
MEMORY ACCESS TIME
IS 375ns.
Memory Cycle Time is 500ns.

Buy an S100 compatible 8K Ram Board and upgrade the same board to a maximum of 32K in steps of 8K at your option by merely purchasing more ram chips from S.D. Sales! At a guaranteed price — Look at the features we have built into the board.

16K FOR $259.00 **8K FOR $151.00**

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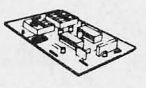
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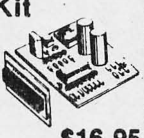
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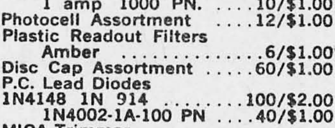
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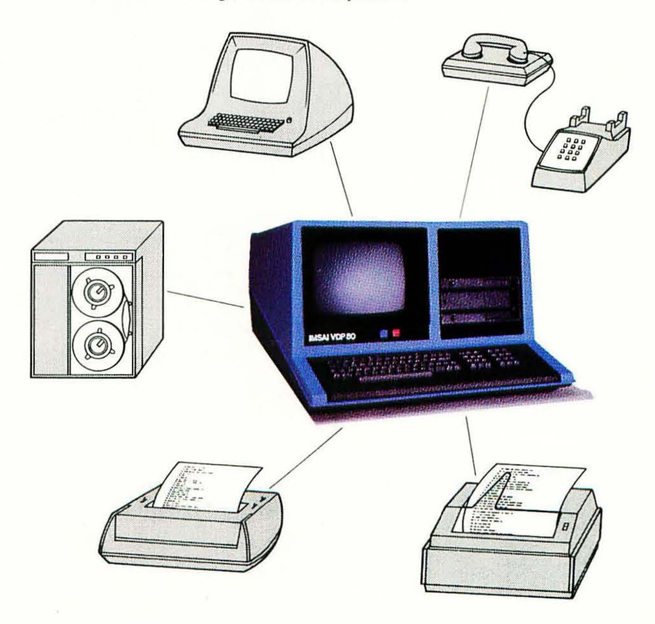
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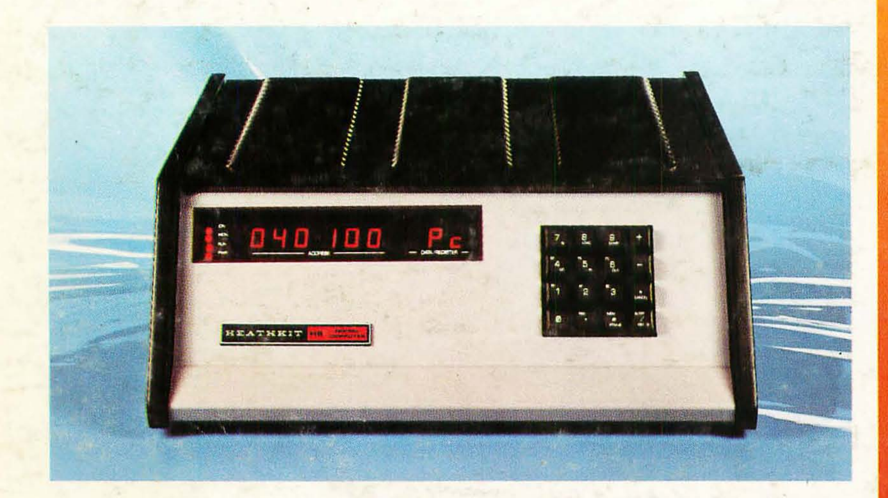
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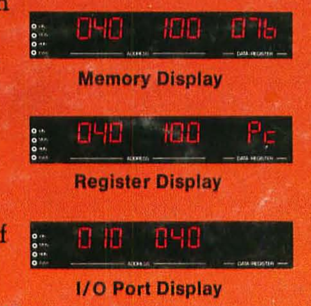
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